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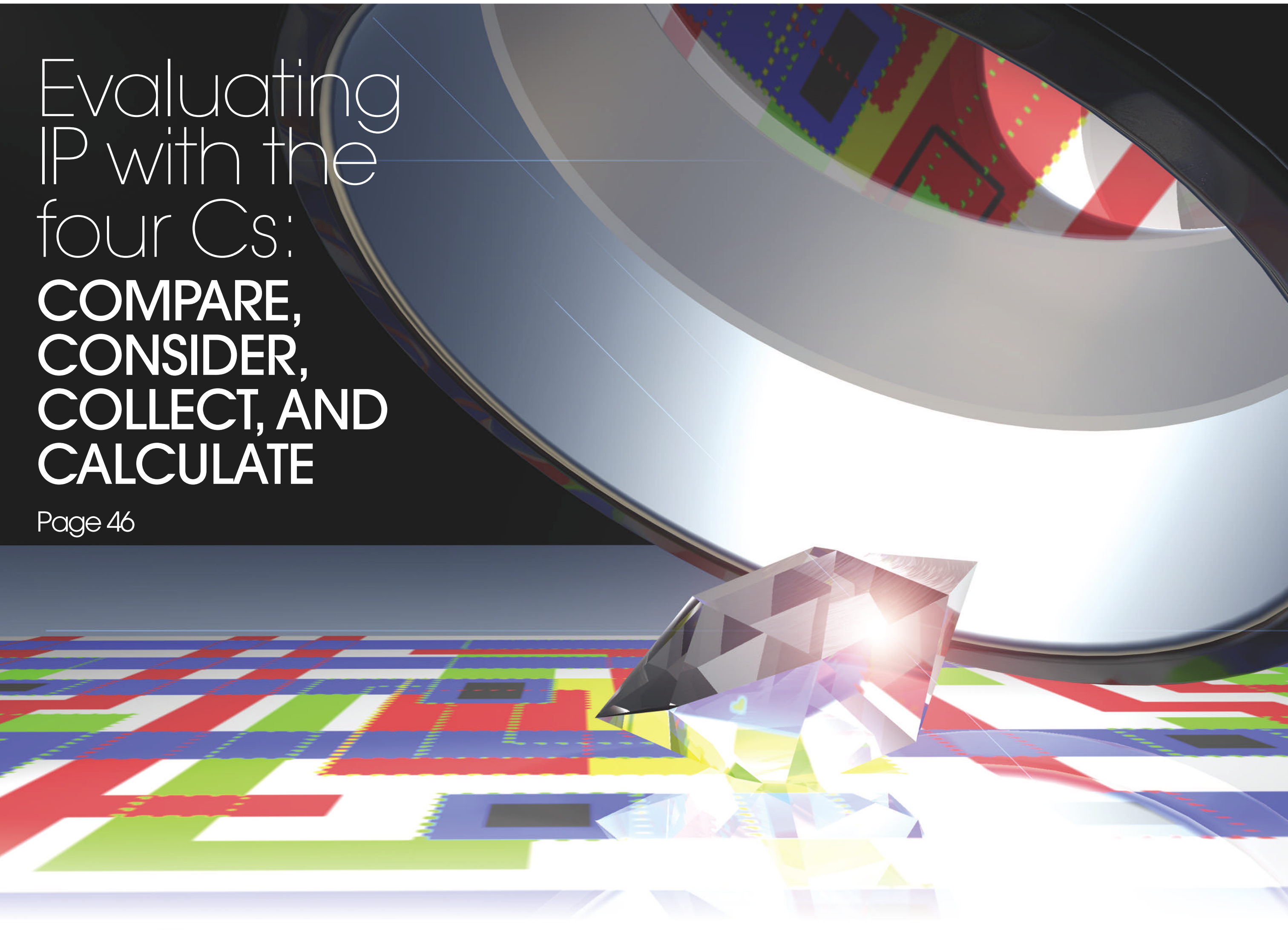

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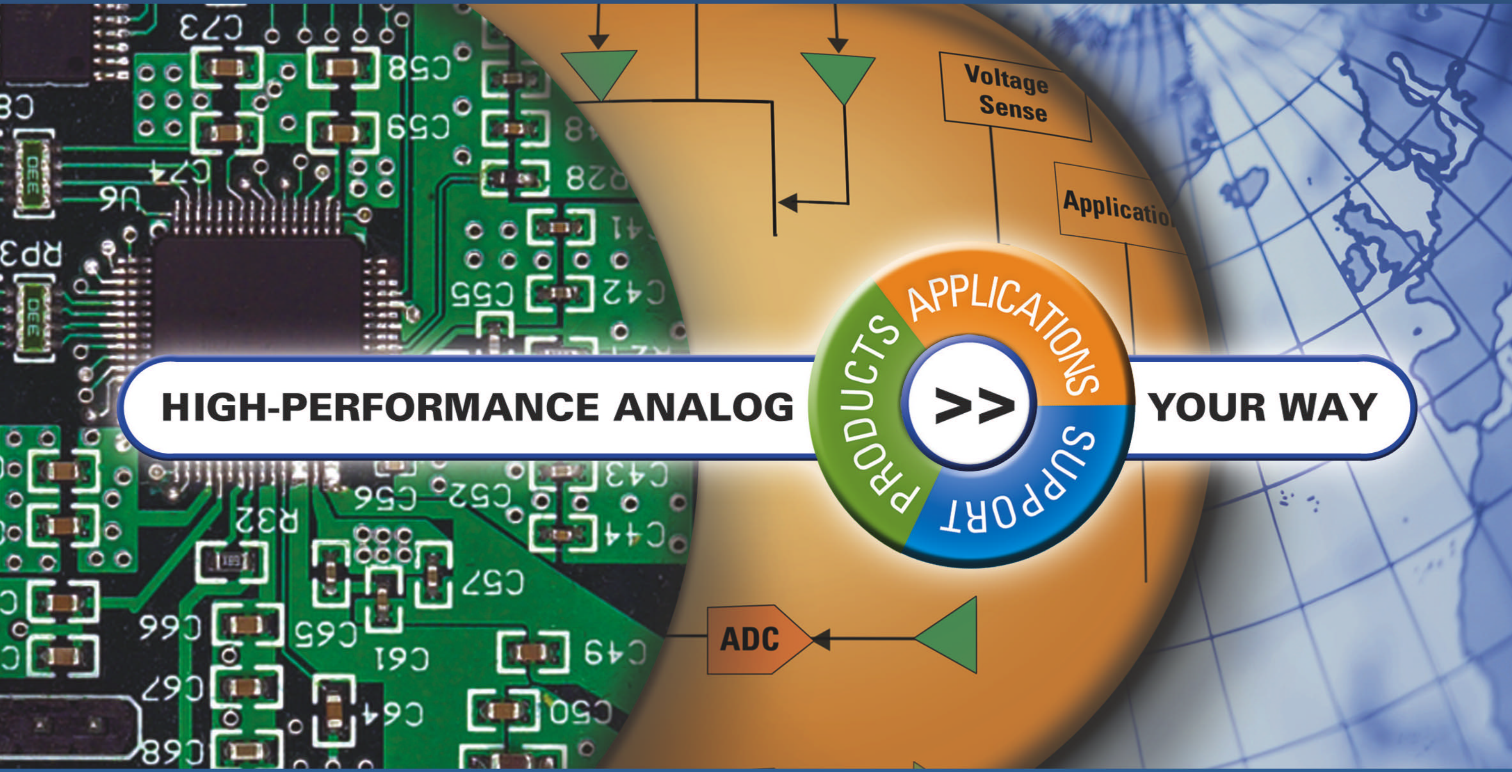

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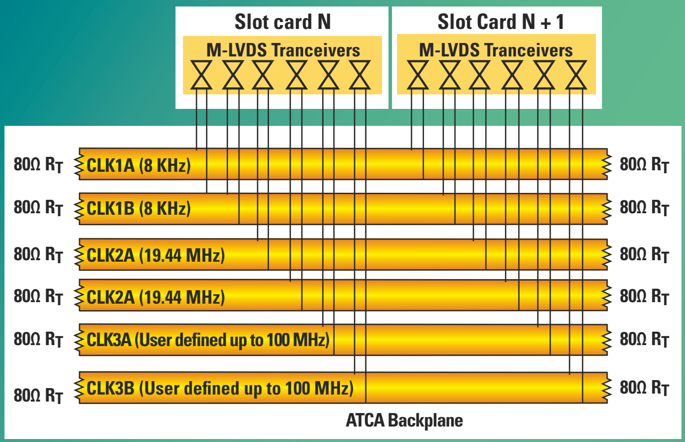

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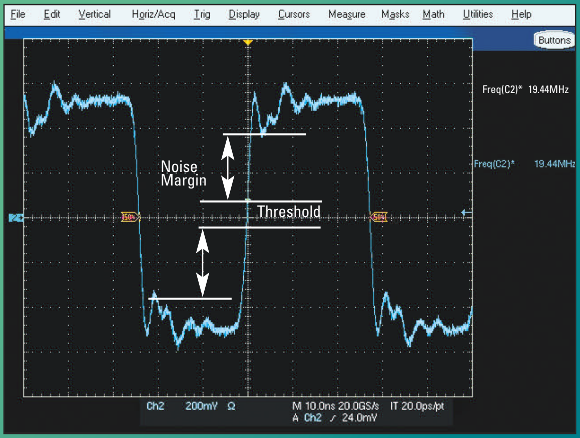

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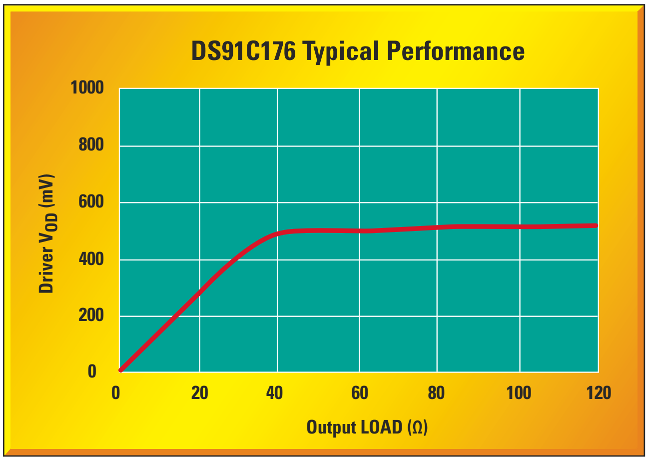

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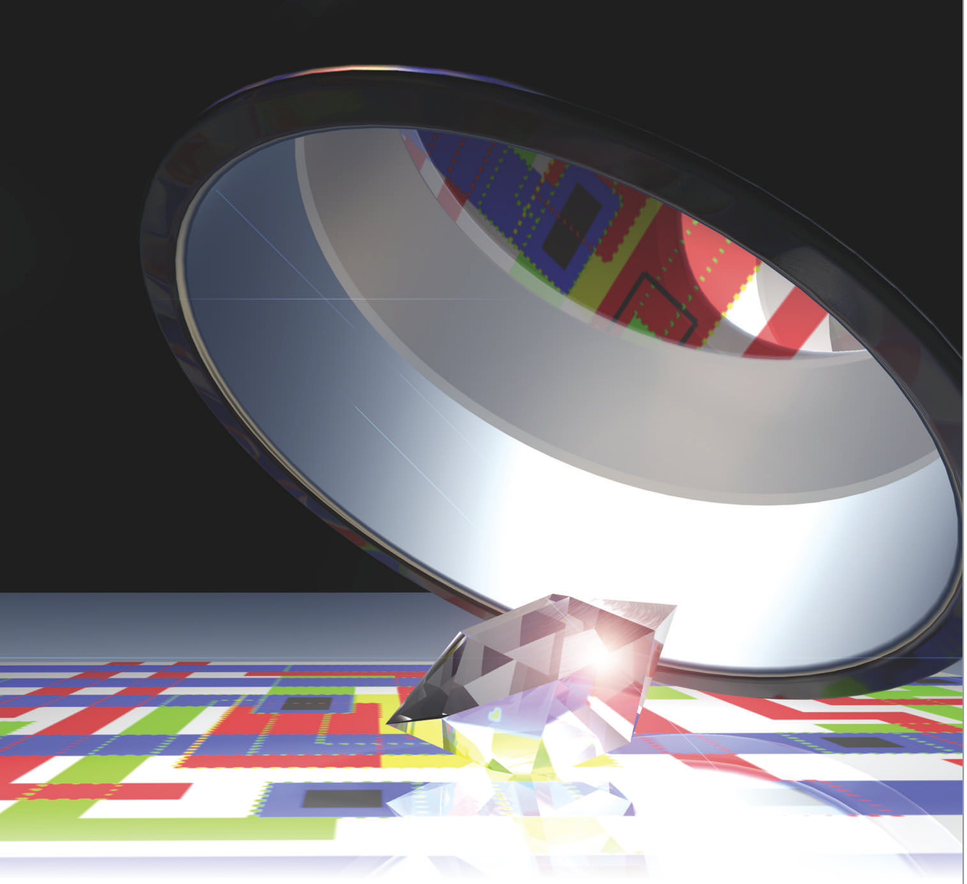
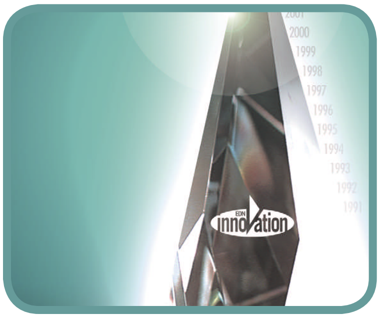


Evaluating IP with the four Cs: compare, consider, collect, and calculate

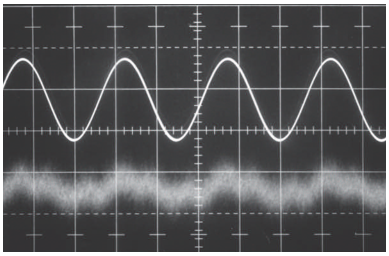
46 Finding quality IP is one of the biggest headaches in IC design. Fortunately, there are a few resources as well as tips and tricks to help designers home in on the best choice. Consider the four Cs: Compare many cores, consider vendor size, collect references, and calculate risks.

by Michael Santarini, Senior Editor



EDN's 2006 Innovation finalists: It's show time!

41 The paparazzi are on standby. The nominees are excited. The ballot is ready. Who will win recognition for outstanding innovation in *EDN*'s 17th annual program honoring engineering excellence? You decide.



Designing instrumentation circuitry with rms/dc converters

57 RMS converters rectify average results.

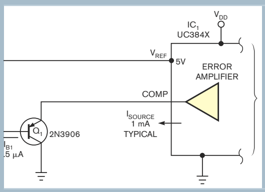
by Jim Williams, Linear Technology Corp

Maximizing EOS and ESD immunity in high-performance serial buses

77 Protecting products from electrostatic hazards may seem to involve black magic, but it doesn't. A layered strategy of defending against the hazards maximizes products' immunity and minimizes the impact on part costs and project schedules.

by Burke Henehan, Texas Instruments Inc

DESIGNIDEAS



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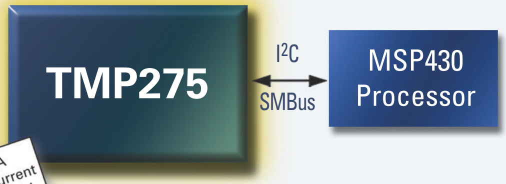

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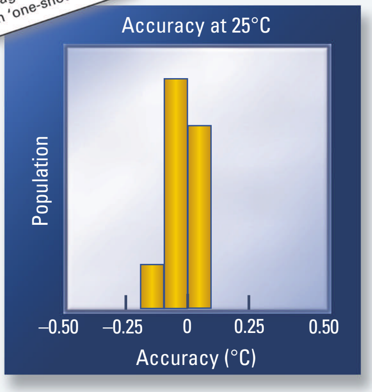

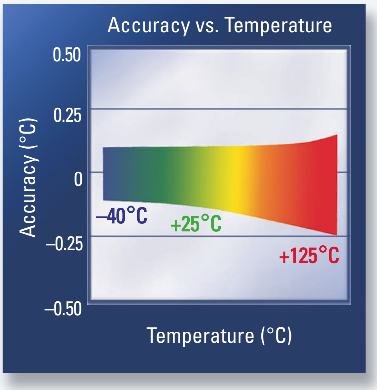

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TMP175	27 Addresses	2-wire	±1.5	2.7 to 5.5	MSOP, SOIC	$0.85
TMP105/ TMP106	World's smallest 1mm x 1.5mm x 0.6mm	2-wire	±2	2.7 to 5.5	WCSP	$0.85
TMP100/ TMP101	Programmable Thermostat/ Alarm	2-wire	±2	2.7 to 5.5	SOT-23	$0.80
TMP121/ TMP122	Fully Programmable Resolution and Thresholds	SPI	±1.5	2.7 to 5.5	SOT-23	$0.99

*Suggested retail price.

*New products are listed in **bold red.***

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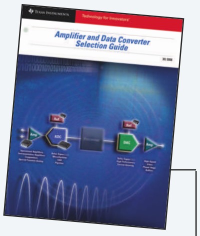
- Package: MSOP-8, SOIC-8
- Price: $1.25 in 1k units



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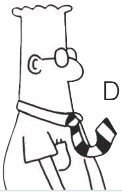

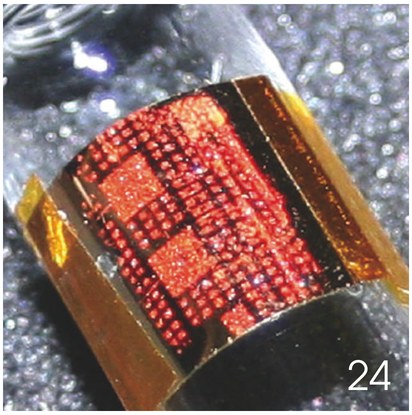

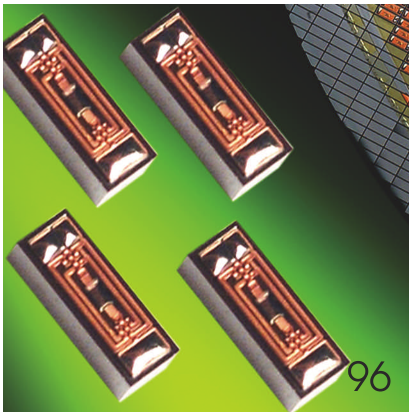

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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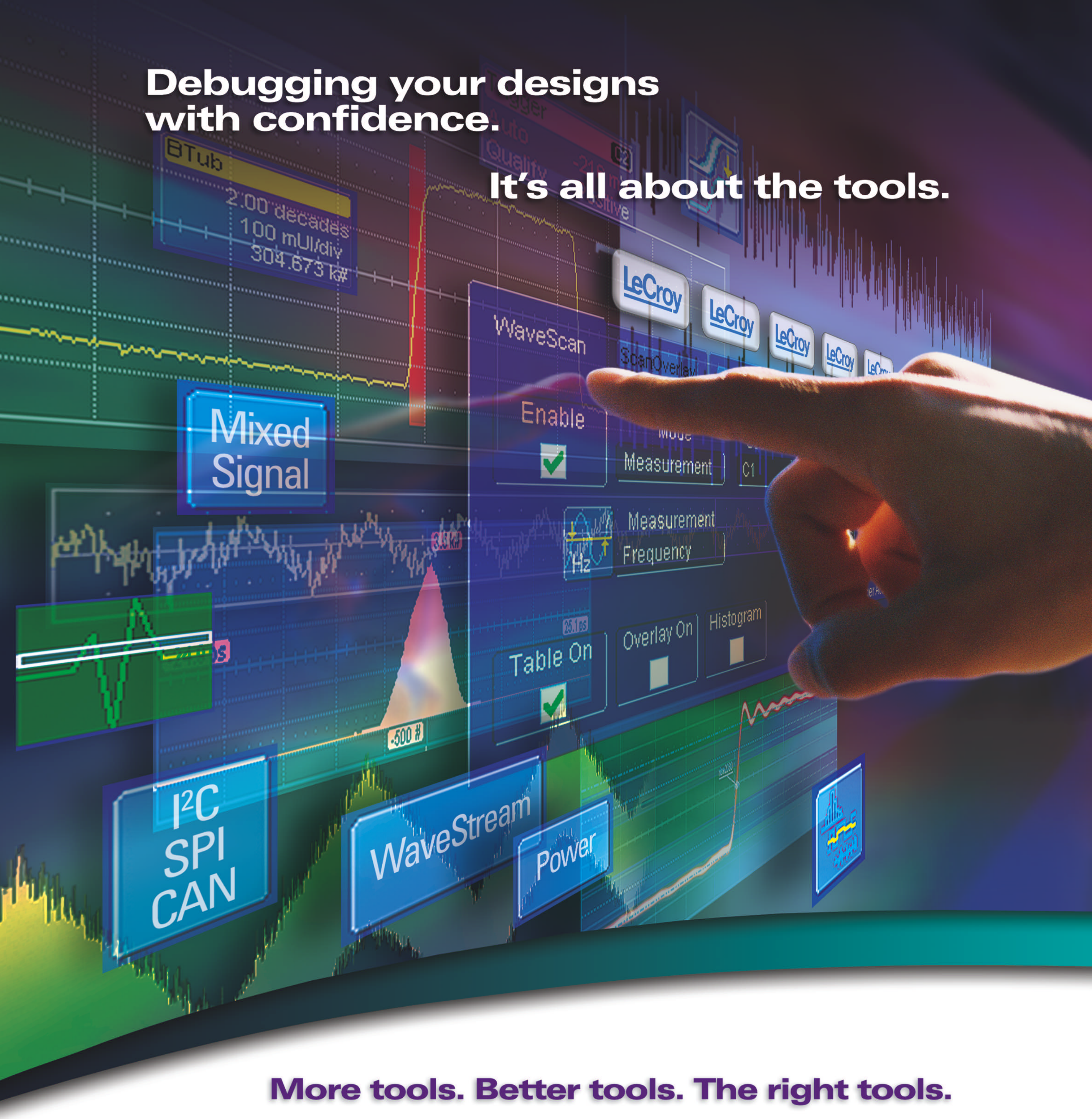
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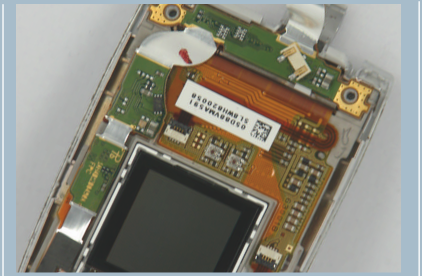

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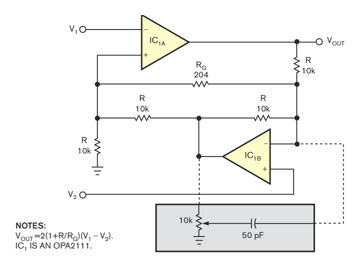

ALL-TIME GREAT DESIGN IDEA

We regularly get requests for copies of articles that predate our online archive (www.edn.com/archive), which contains everything from 1994 to the present. But a 1986 Design Idea, "Use dual op amp in an instrumentation amp," has always generated more requests than normal. We aren't sure how readers know about this Design Idea, but its enduring popularity recently led us to publish it again, and it's now available online at this address:
→ www.edn.com/article/CA6406733

THE TOP 10 ARTICLES OF 2006

EDN's Microprocessor Directory tops the list of your favorite articles of 2006, but blue-laser DVDs, circulating currents, ground bounce, Mathcad, hazardous voltages, and CMOS inverters also make appearances. See the complete list, plus a list of the most popular archived articles:
→ www.edn.com/article/CA6406707

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BY MAURY WRIGHT, EDITOR IN CHIEF

Has Jobs lost his magic?

Immediate product availability has been the most impressive aspect of Apple's performance in its resurgence this decade. When Steve Jobs demonstrated a product such as the Mac mini at Macworld Expo (www.macworldexpo.com), eager Apple fans would be able to buy the toy the next day. And generally, Apple has amazingly kept details of upcoming products a secret from the bulk of the industry. But judging by the announcements at last month's Macworld Expo in San Francisco, Jobs and Apple are struggling a bit in the increasingly converged world in which partners really matter.

The long-awaited Apple iPhone finally arrived, but fans will have to wait until summer to buy the iTunes-compatible phones from Cingular. I realize that the delay may have more to do with Cingular than with Apple, but that's the point. In a converged world, Jobs must learn, and perhaps he has, that he can't call all the shots. Unless Apple builds out its own cellular network, the company will be at the mercy of the carriers that move excruciatingly slowly at qualifying new devices. Rightfully, the carriers are terribly afraid of customer-support issues and product returns.

The iPhone itself looks well-designed from the user-interface perspective. Of course, users of products such as the Treo have been using a touch-sensitive display for some time, and Jobs clearly overhyped the innovations in the user interface. But I expect the iPhone will generally offer among the best user interfaces.

But my questions on the design of the phone start with the features of the baseband and radio. Cingular already offers a number of UMTS-capable phones, including the HTC 8525, which also features a screen to match the iPhone as well as a full keyboard. At launch, the iPhone will support only the slower EDGE (enhanced-data-for-GSM-environment) network. The HTC weighs a couple of ounces more than the iPhone but is more capable and available now. It matches the Wi-Fi offering of the iPhone and really comes up lacking only in iTunes support—and that matters only if you've bought a library of iTunes content.

Jobs and Apple are struggling a bit in the increasingly converged world in which partners really matter.

Who made the decision to launch the iPhone with only EDGE support? Why didn't Apple announce the phone earlier if it was an EDGE device? Does Apple bluster about voice messages even matter with the relatively slow EDGE network? Without question, the dynamics of working with a partner aren't among Apple's strengths.

Apple performed only slightly better with the Apple TV announcement. Again, eager fans will wait, although perhaps only a month, to buy the product. When Apple hinted at the product last summer, my guess was that the ability to stream video would be the obstacle to it. But Apple looks ready to launch with support for the legacy 802.11g Wi-Fi network and to offer prestandard 802.11n capabilities.

I'm still not sure whether Wi-Fi is suitable for home-video distribution. I'm researching that topic, yet again, for an update on home-video networks due next month. The Apple TV product does have characteristics that may not stress the video network. The content, presumably coming mostly from iTunes, is relatively low-resolution and, therefore, not bandwidth-intense. Moreover, the Apple TV application can buffer content to accommodate fading in the 802.11 signal.

I'm sure Jobs will boast of being the first to solve the home-video-distribution problem, just as he takes credit for the compressed-digital-music revolution. Again, he will have stretched the truth. Apple TV doesn't approach the level of the problem that carriers face in trying to deliver high-definition-video streams around a home with no buffering or latency.

What I hope I'm seeing with the latest from Macworld Expo is an Apple that will be forced to embrace more open standards. The lessons the company is learning in the handset business will surely hit home. Despite Jobs boasts to the contrary, it looks like iTunes music sales are stalling. The same will happen with video. On the other hand, a more open approach to the Apple codec and digital-rights management might ultimately serve the company much better than the current stance that limits content to Apple hardware. **EDN**

Contact me at mgwright@edn.com.

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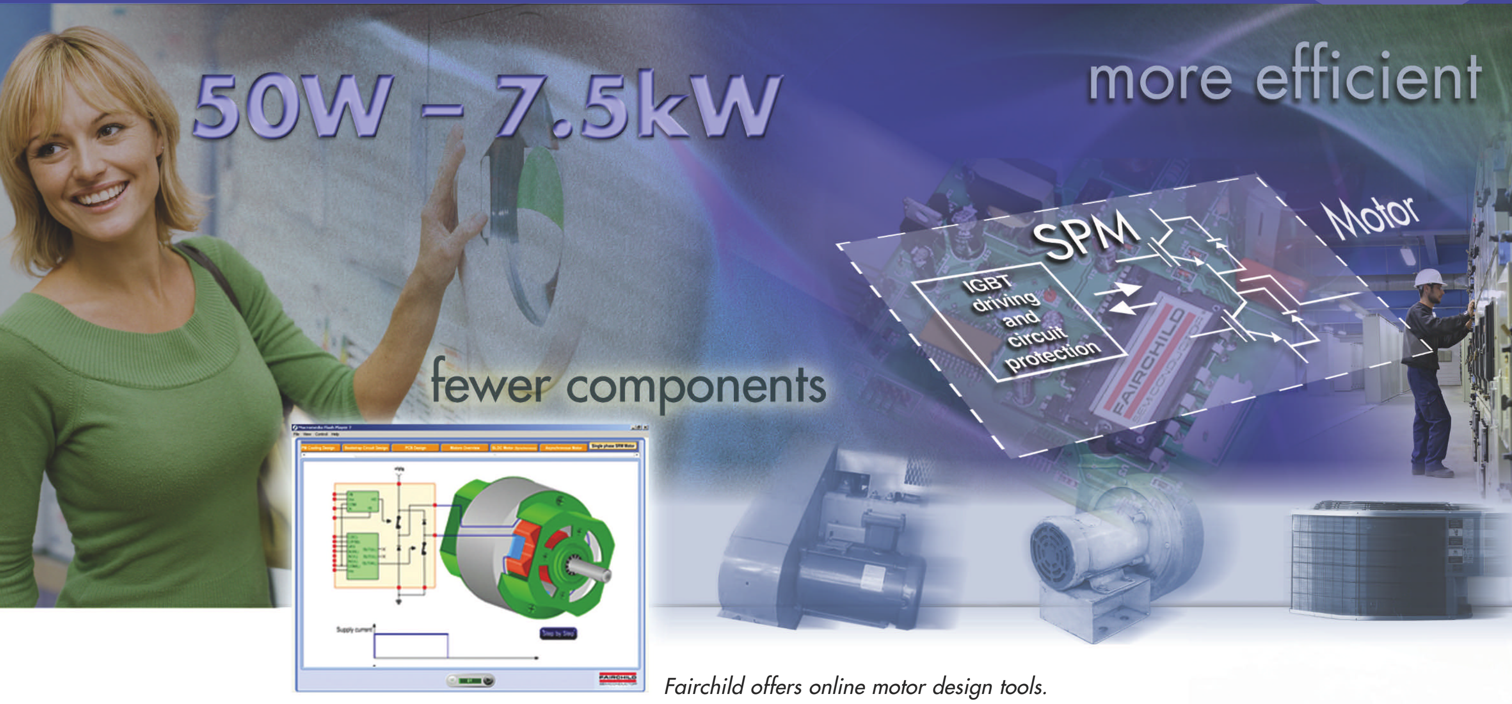
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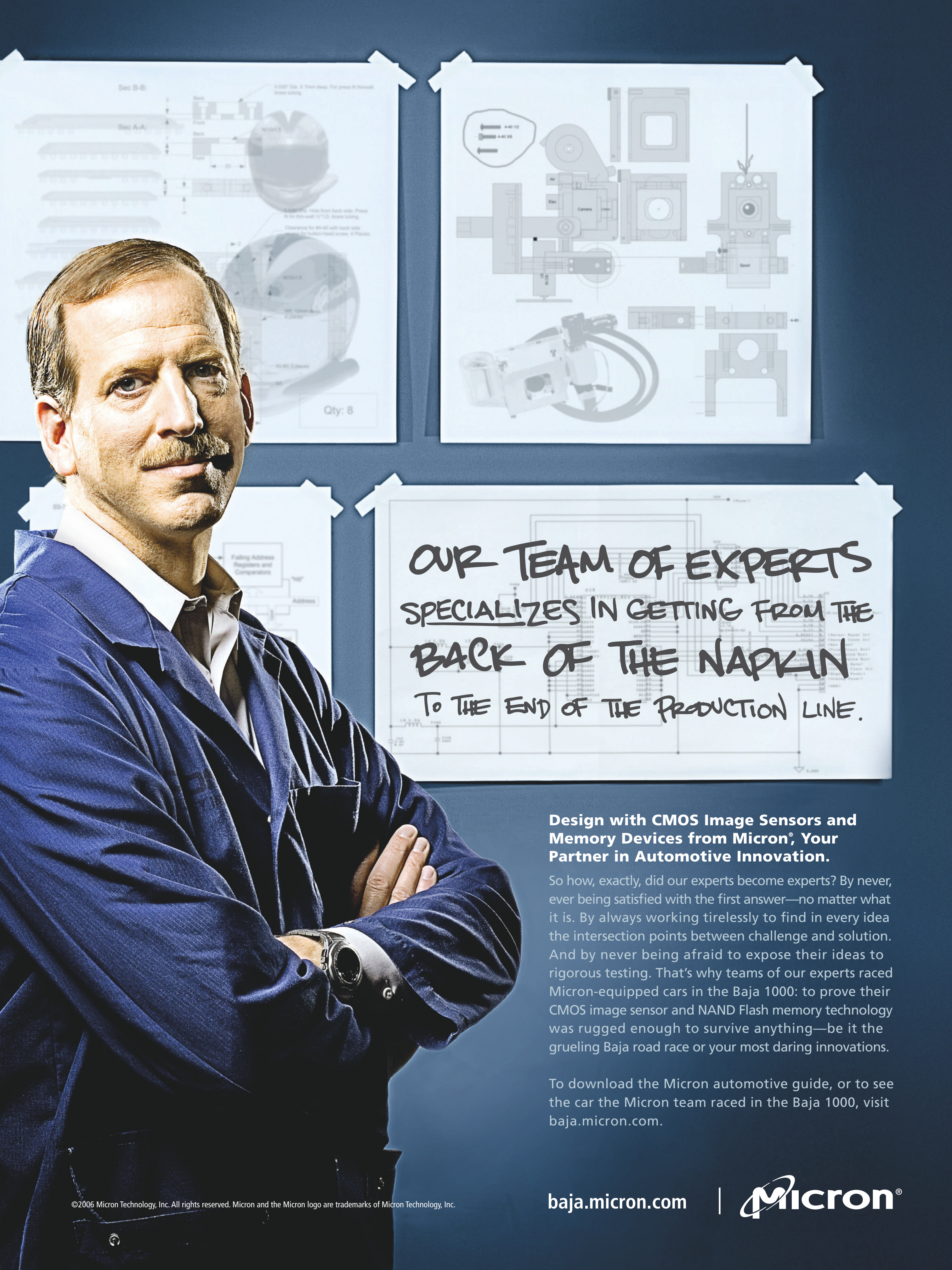
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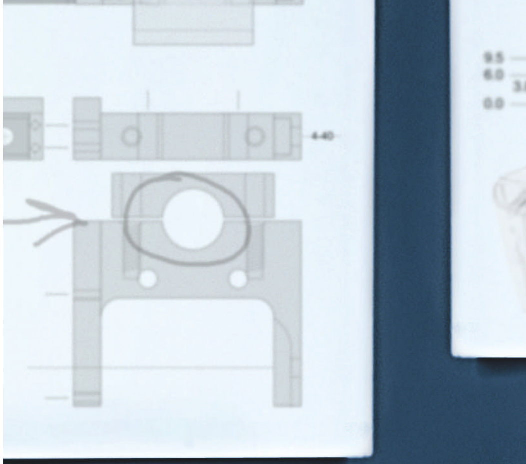

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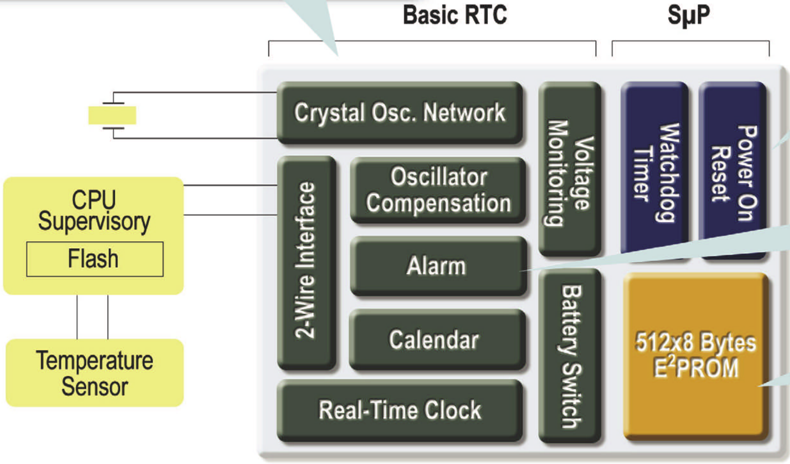

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Integrated 4k Bytes of E^2PROM memory reliable for >2,000,000 write cycles eliminates external device.

800nA General Purpose Real-Time Clock Selector Table

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			POR	Wdg Timer	$\overline{IRQ}$	F_{OUT}	V_{TRIP} for Rest/Bat Switch	Package
ISL12026	512 X 8	2	N	N	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12027	512 X 8	2	Y	Y	$\overline{RESET}$		5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12028	512 X 8	2	Y	Y	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP
ISL12029	512 X 8	2	Y	Y	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP

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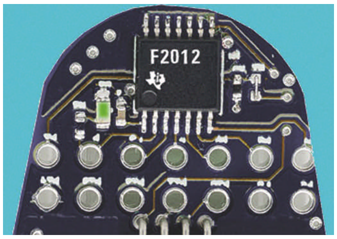
EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Target boards extend USB-development tool

Expanding the flexibility of its popular eZ430 stick-based development and emulation tool, Texas Instruments recently announced two target boards to support low-power industrial, medical, and consumer applications, including metering, portable instrumentation, and intelligent sensing.



The T2012 target board from Texas Instruments extends the eZ430 USB-stick development tool to include the MSP430F2012 ultralow-power microcontroller.

The $20, self-powered eZ430 connects to a standard PC USB port and requires no extra cables or power supplies. The eZ430 tool includes a free IAR (www.iar.com) Kick Start Embedded Workbench IDE (integrated development environment) containing a debugger, an assembler, and a C compiler. The USB stick contains an emulation-interface board and an easily removable MSP430F2013 board that you can replace with the new target boards. At $10 for a pack of three identical target boards, the new T2012 features the ultralow-power MSP430F2012 microcontroller, which integrates a high-performance, 200k-sample/sec, 10-bit ADC.

Another eZ430 target board, the MSP-Mojo from Quickfilter Technologies, features a 512-tap, embedded, single-channel precision digital-filter chip for precision digital-filtering applications, including vibration monitoring, audio filtering, and medical-patient monitoring. The MSP-Mojo target board is available through authorized distributors for $39.95.

—by Warren Webb

▷**Texas Instruments**, www.ti.com/ez430.

▷**Quickfilter Technologies,** www.quickfiltertech.com.

FEEDBACK LOOP

"'Energy harvesters' and other types of relatively 'exotic' alternative-energy sources could greatly benefit from using supercapacitors as intermediate energy storage. ... The bottom line: It is absolutely clear to me that supercapacitors are going to revolutionize the electronics and power industries ... in the very near future."

—Alexander Bell, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6399099. Add your comments.

RTOS upgrade adds USB 1.1 and 2.0 support

Green Hills Software has upgraded its μ-velosity RTOS (real-time operating system) to include support for a PC-compatible file system, a wear-leveling and fault-tolerant flash-device manager, a USB 1.1- and 2.0-device-class framework, and the GHNet TCP/IP (Transfer Control Protocol/Internet Protocol) networking suite. The μ-File file system supports MS/DOS and flash-file formats, and developers can access it through standardized interfaces, such as POSIX (Portable Operating System Interface), C-standard I/O, and C++-I/O streams.

The μ-USB-device management includes a framework and API for managing device connectivity for a variety of device types, including mass-storage products, such as USB-memory sticks. The GHNet TCP/IP-networking suite includes protocol support for TCP, UDP (User Datagram Protocol), and SNMP (Simple Network Management Protocol).

Version 2.2 of the RTOS can fit into a ROM footprint as small as 1600 bytes and a RAM footprint as small as 1 kbyte. Its boot time is less than 1500 cycles, and it supports service-call times as low as 30 cycles. The μ-velosity API is upward-compatible with Green Hills' Integrity RTOS as an upgrade path. Version 2.2 of μ-velosity is now available, and it supports the ARM, Power Architecture, ColdFire, MIPS, and Blackfin processor families. Prices for royalty-free licenses start at $9500.**—by Robert Cravotta**

▷**Green Hills Software**, www.ghs.com.

MLC and SLC NAND-controller core, development software emerge

Denali Software Inc is expanding its implementation-IP (intellectual-property) portfolio with the recent introduction of a new controller core for MLC (multilevel-cell) and SLC (single-level-cell) NAND devices. Over the years, Denali has built a solid reputation by offering memory models, a type of verification IP, but the company a few years ago also started building a portfolio of implementation IP in what it calls its Databahn. In the memory market, the company has to date offered a PCI Express core, a DDR-DRAM-controller core, and a NAND-controller core for SOCs (systems on chips) controlling Samsung's (www.samsung.com) OneNAND hybrid NAND.

Now, the company is adding its Databahn NAND-flash controller to the Databahn portfolio. This controller core, says Raj Singh, Denali's director of business development, targets controlling a broader range of NAND devices in a variety of architectures, including XIP (execute in place), shadow, and store and download. Singh notes that Denali is providing not just the RTL (register-transfer-level) core, which has fewer than 100,000 gates, but also the Spectra NAND-flash-management software.

The Spectra software allows users to adjust the controller to control specific NAND architectures and includes optimal-wear-leveling algorithms, power-loss recovery, and bad-block management. The Spectra tools also include multibit-ECC (error-correction-code) algorithms that allow users to program 8-bit ECC into devices. Today, only systems requiring the highest levels of security and reliability call for 8-bit ECC. Singh notes that, as the industry moves toward full boot-from-NAND architectures, thus eliminating the need for NOR devices, designers will most likely need to use more ECC in their designs. This ECC stops both write and read errors in NAND devices, which are inherently less reliable but ultimately less expensive than NOR devices.

The ECC features also allow users to ensure that their SOCs can work with MLC and SLC NAND devices. Denali offers several licensing options for the core, including one-time licenses and multiple-year subscriptions to royalty-based licenses.

—by Michael Santarini

▷**Denali Software Inc**, www.denali.com.

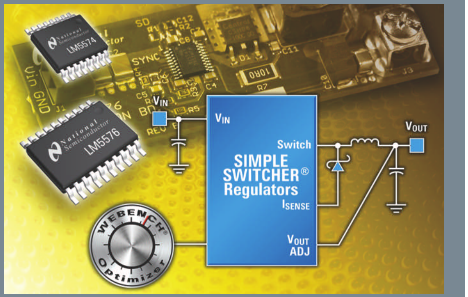
VOLTAGE REGULATORS EMPLOY ECM

National Semiconductor's new 6 to 42V LM25574/5/6 and 6 to 75V LM5574/5/6 series of Simple Switcher voltage regulators output 0.5, 1.5, and 3A. The new parts operate at 50 kHz to 1 MHz. Unlike competitors' switchers, derating below 1 MHz occurs only with step-down ratios beyond 36 to 2V. The Simple Switchers also use a novel method to emulate the current in the inductor without inserting an efficiency-robbing sense resistor or using the dc resistance of the inductor, which varies from design to design, from part to part, and over temperature. ECM (emulated-current mode) senses the current in the freewheeling diode during the leisurely off-time period, providing better transient response. This clever feature is one of the reasons the new line of parts needs 16 or 20 pins, rather than five, as its predecessor had. The anode of the freewheeling diode connects to the part, so the part can measure the diode current with an accurate and simple low-side sense circuit.

Using the Simple Switchers and National Semiconductor's Webench online-design tool, you can optimize designs for operating frequency, efficiency, soft-start time, board size, and transient response. The designer needs only to enter the required parameters, and the Webench tool calculates a BOM (bill of materials), runs a Spice simulation, and does a thermal analysis of the design. Webench now has a large, intuitive knob that lets designers choose between efficiency and board size.

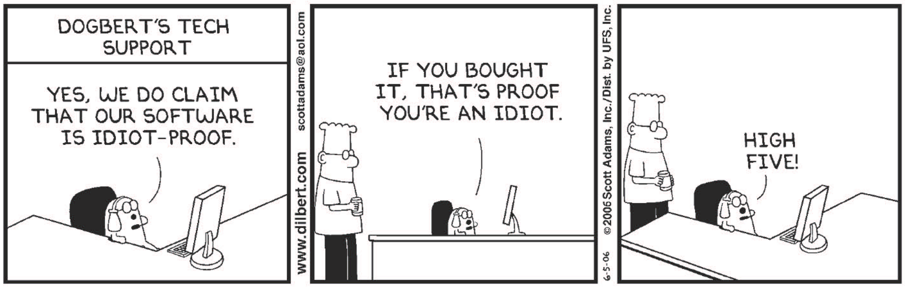
The 0.5 and 1.5A parts come in TSSOP-16 packages, and the 3A parts come in TSSOP-16 packages. Prices ranges from $1.35 to $2.90 (1000). Demo boards and Built-It boards for Webench are available.—by Paul Rako

▶**National Semiconductor,** www.national.com.



The new Simple Switchers operate at 50 kHz to 1 MHz.

DILBERT By Scott Adams



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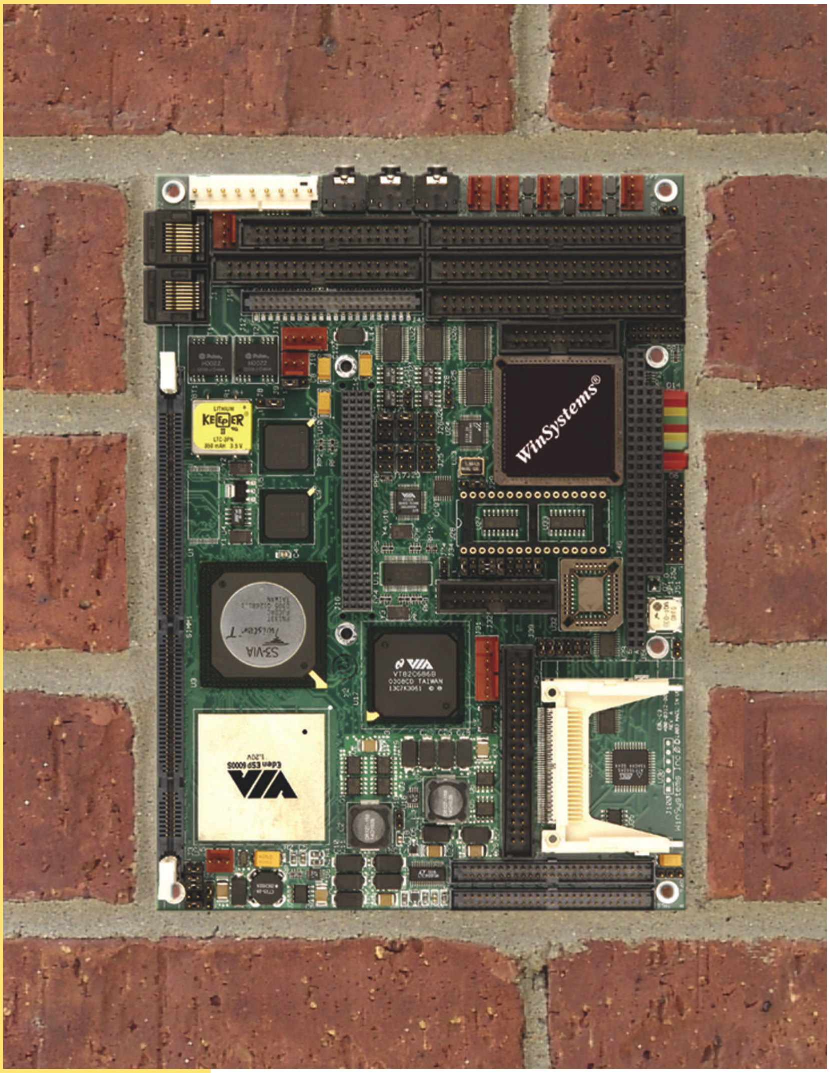

The EBC-C3 embeds 9 different functions to provide a processor- and I/O-intensive solution. It operates over a -40° to +85°C temperature range without the need of a fan, making it ideal for embedded applications such as robotics, MIL/COTS, transportation, pipeline, and machine control.

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Lithium-ion advancement improves safety and energy density

Matsushita, which most people know better by its brand name, Panasonic, recently announced an advancement in lithium-ion cells that the company claims will make lithium-ion-battery packs safer and will slightly increase energy density, or the battery's capacity for power. These features are important for lithium-ion-battery packs, which commonly find use in laptops, cell phones, and other digital products.

The lithium-ion 18650 cell, which gets its name from its dimensions of approximately 18 mm in diameter by 65 mm long, has been around for about 15 years. During that time, the cell's capacity has increased from about 1.2 Ahr in the early '90s to the 2.9 Ahr of Panasonic's new cells.

According to Rory Pynenburg, PhD, applications-engineering manager at lithium-battery-pack-design house Micro Power (www.micro-power.com), battery manufacturers have been cramming more battery-active materials into the same cell dimensions. To achieve that task, they've had to compromise the thickness of the separator layer between the anode and the cathode. The separators are polyolefin, typically a polyethylene with about 40% void volume. "The downside of using polyethylene is that, at about 93 to 98°C, the separator softens, and it can allow penetration by contaminants, leading to a short," says Pynenburg. "In pure polyethylene, it will start off with a pinhole penetration and then rapidly widen out, increasing the anode-to-cathode contact area, and you end up in a thermal-runaway situation." In layman's terms, this "situation" translates to a fire.

But the need for greater energy density in lithium-ion batteries only increased during the '90s. When cell manufacturers increased the thickness of the battery-active materials and, thus, the cell's energy density, the trade-off was to make that separator thinner, going from a 25-micron to a 20-micron separator, with the corresponding increase in the probability of a thermal-runaway event.

In retrospect, it seems inevitable that Sony (www.sony.com) would be the manufacturer to experience the massive battery recalls—not because of any quality problems, but because its dominant position as the major supplier in the battery-cell market allowed the numbers to catch up to it. When you manufacture millions of cells, a failure rate of one in 200,000 becomes significant.

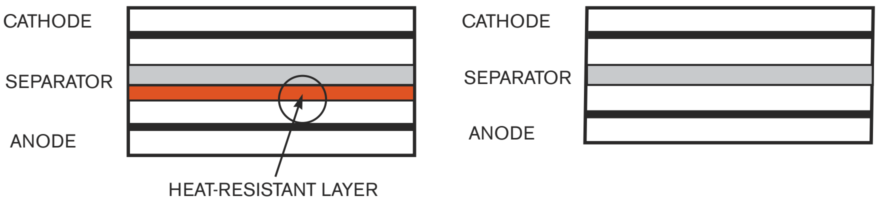
> “It's going to be a nice parachute to have.

According to Pynenburg, Panasonic's improvement was the introduction of ceramic material, a metal oxide, that goes between the separator and the electrodes—the anode and cathode. "It's shrouded in a bit of mystery as to whether [Panasonic is] coating it onto the electrodes or onto the separator," he says. "But the metal oxide does greatly increase the thermal stability, so that if there is a penetration through the separator, it stops there, and you don't get the thermal-runaway situation." The polymeric separator is still present, but Panasonic has added a heat-resistant layer.

Pynenburg believes that the technology will be valuable to Panasonic and its customers. Again, because of the relatively low defect rates, the advantages of the new technology will probably be invisible to most of Panasonic's customers, but, as Pynenburg says, "When its needed, it's going to be a nice parachute to have."

—by Margery Conner

▷**Panasonic**, http://panasonic.net.

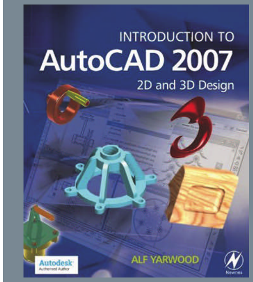


Panasonic has added a heat-resistant layer to a lithium-ion cell (left), which conventional batteries (right) lack.

02.01.07

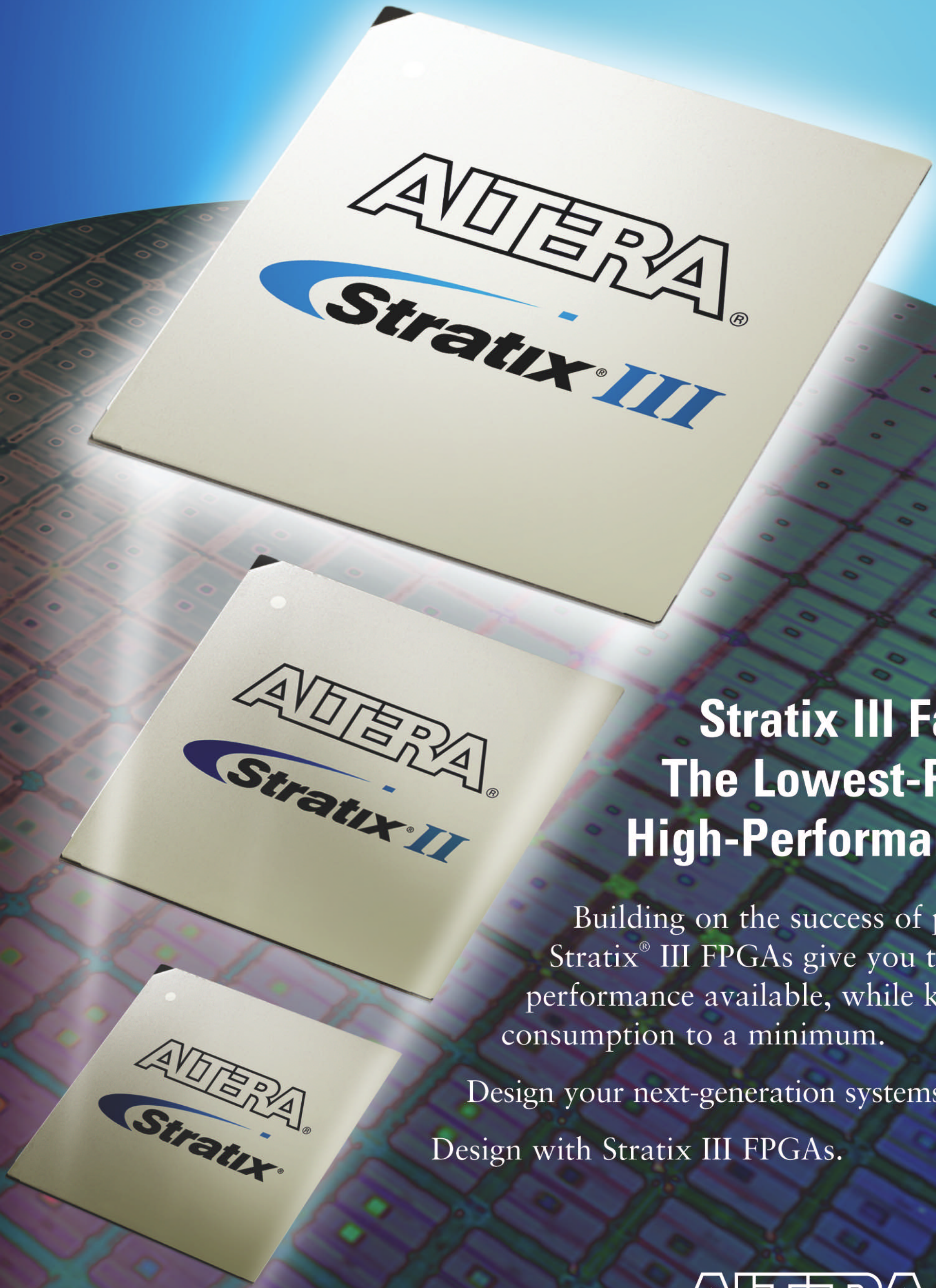
WHEN ELECTRONIC DESIGN ISN'T ENOUGH

Most EEs work comfortably with electronic CAD/CAE tools and don't need to venture into mechanical design. However, if you work with electromechanical devices, you may need to gain familiarity with mechanical-CAD tools, too. *Introduction to AutoCAD 2007: 2D and 3D Design* (Newnes/Elsevier ISBN 0-7506-8154-3, 2007) by Alf Yarwood provides step-by-step instruction for using AutoCAD 2007. The book's generous use of full-color figures makes it easy to follow the exercises. Unlike some step-by-step books, this one discusses menu options in addition to those you are using in the exercise, so that you can leave the path that the exercise provides. This approach makes the text useful as a reference, too, and especially handy for those of you who might not regularly use mechanical-CAD tools. The 346-pg, $39.95 book gives equal time to both 2- and 3-D design.



—by Margery Conner

▶**Newnes/Elsevier,** www.newnespress.com.



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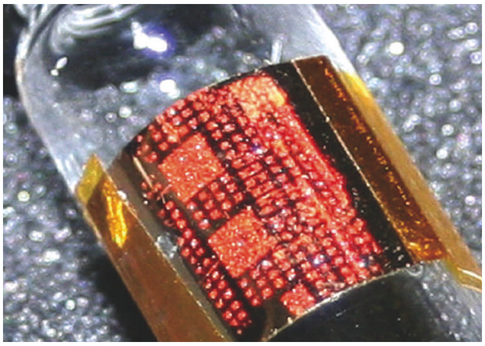


A flexible substrate carrying arrays of monocrystalline transistors wraps around a glass vial.

RESEARCH UPDATE

BY RON WILSON

New direction may be breakthrough for flexible electronics

The technology of printing organic transistors onto a flexible substrate to create plastic circuits has existed for some time now and has found applications in the few instances in which flexibility is mandatory but speed, density, and energy efficiency are not important. The limiting factor in all these dimensions has been the organic-semiconducting material itself; all of the previously explored materials, although flexible and compatible with simple offset, ink-jet, or laser printing, have low carrier mobility.

However, researchers at Stanford University and the University of California—Los Angeles have conducted a series of experiments that may constitute a breakthrough (**Reference 1**). Instead of printing an organic semiconductor directly onto the substrate in an amorphous state, the new technique uses a patterned polymer stamp to print a crystal growth agent, OTS (octadecyltriethoxysilane), onto the desired transistor sites. The technique then introduces a vapor containing the intended organic-semiconductor material, and single-crystal structures grow where the growth agent is present.

Researchers have demonstrated monocrystalline transistors of rubrene and Buckyballs. The devices exhibit the high-carrier-mobility characteristic of single-crystal transistors and, hence, acceptable performance for many applications. Researchers have built devices with dimensions of microns, and experiments have shown that repeated flexing does not impair the transistors' electrical characteristics. Now, the researchers are turning their attention to controlling the orientation of the crystal that forms on the growth agent and improving the electrical contact between the crystal and previously printed metal electrodes.

▷ **Stanford University**, www.stanford.edu.

▷ **University of California–Los Angeles**, www.ucla.edu.

REFERENCE

1 Briseno, Alejandro L, et al, "Patterning organic single-crystal transistor arrays," *Nature*, Dec 14, 2006.

RESEARCHERS INCH FORWARD ON PHASE-CHANGE MEMORY

02.01.07

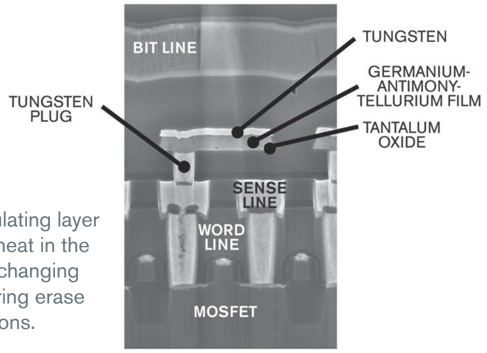
Two reports at the International Electron Devices Meeting last December indicated gradual progress on the considerable challenges of making phase-change memory into viable products. One, from Hitachi and Renesas, involves containing heat in the phase-change film long enough to effect the phase change. The other, from IBM (www.ibm.com), Qimonda (www.qimonda.com), and Macronix (www.macronix.com), describes fabrication of working phase-change memory cells small enough for use at the 20-nm-process node and considerably faster in switching than today's flash-memory cells.

The Hitachi work addresses a problem that a previous breakthrough created. Last year, the two companies demonstrated a germanium-antimony-tellurium film that showed significantly reduced current requirements for changing phase. But the heat that these low currents generated easily escaped through the contact into the sense transistor before the phase change completed. So, this year, the two companies reported on successful use of a tantalum five-oxide film between the phase-change film and the contact, permitting current to flow but reducing heat loss.

The IBM research demonstrated 3×20-nm bridges of a doped germanium-antimony alloy–the composition of which resulted from a major materials-research project in its own right, according to the companies. They used the bridges to fabricate memory cells–small enough for use at the 20-nm-process node–that program at less than half the write power that today's flash cells use and that could write in about 1/500th the time that flash requires. Neither team of companies is claiming anything close to a production device. But, one by one, materials science seems to be crushing the barriers.

▶ **Hitachi,** www.hitachi.com.

▶ **Renesas,** www.renesas.com.



An insulating layer keeps heat in the phase-changing film during erase operations.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Microcontroller cores focus on video decoding

Tensilica's Xtensa and LX2 architectures let you invoke a range of options for processor-core functions and peripherals and create custom instructions. The company's design-tool package automatically generates a custom compiler that matches your specification. New versions of both cores now come with the option to add on-the-fly error correction to handle soft-memory errors. Tensilica recently began to offer preconfigured versions of its cores for specific application domains under the Diamond Core label. Although the point of the architecture is configurability, Tensilica says that it often makes first contact with a potential customer's project when that project has reached the core-selection stage, according to Marketing Vice President Steve Roddy. Hence, Tensilica offers a range of preconfigured cores targeting popular applications.

Now, the company has added to that series with a media processor that it intends for power-efficient compressed-video decoding in portable products. The design generates a twin-core structure using the Xtensa architecture. One core, an SIMD (single-instruction-multiple-data) pixel processor, performs computationally intensive detail processing of the image data. The other core, a dual-issue VLIW (very-long-instruction-word) block, handles the stream processing and control functions for video decoding. The result is an IP (intellectual-property) block that handles all aspects of the video-decoding function and that is completely software-programmable.

The 388VDO processor handles eH.264 Main Profile D1/Standard Definition with a predicted power demand of 34 mW and clock rate of less than 200 MHz if you use TSMC's (Taiwan Semiconductor Manufacturing Co's, www.tsmc.com) 90G 90-nm process. "We think it is currently the only main-profile H.264 solution in shrink-wrap form [hardware IP plus software] available," Roddy says. The core will implement CABAC (content-adaptive binary-arithmetic coding) that delivers improved image quality in H.264.

–by Graham Prophet, *EDN Europe*

▷ **Tensilica**, www.tensilica.com.

Handset availability may slow interest in converged VOWLAN/cellular services

Consumers are enthusiastic about the billing and service plans that converged VOWLAN (voice-over-wireless-local-area-network)/cellular services could provide, but the availability of suitable handsets could cause the market to develop slowly, reports In-Stat.

"There is unprecedented interest in 'home-zone' pricing, which offers unlimited local and domestic long-distance calls for a single flat fee when the customer uses a home Wi-Fi access point or a Wi-Fi hot spot," says David Chamberlain, an analyst an In-Stat. "This concept is just one of the possible services from converged VOWLAN/cellular technology."

—by Vinod Kataria, *EDN Asia*

▷ **In-Stat**, www.instat.com.

REFLECTIVE-DISPLAY TECHNOLOGY OPERATES IN ALL LIGHT LEVELS

Start-up Liquavista is proposing a new display technology as the ideal approach for mobile and portable displays. The effect, which the company intends to exploit, is not new, but no one has previously developed the approach to construct a display technology for volume production. The phenomenon, "electrowetting," uses a cell (for displays, a pixel) containing two immiscible liquids: oil and water. Applying a voltage to the cell changes the state of the surface, over its active area, from hydrophilic to hydrophobic. In one condition, the oil lies in an even layer across the cell; in the other, electrical charges and surface-tension effects repel it to accumulate in one corner of the pixel cell. Load the oil with a colored dye or an opaque material, and you have the basis of an optical switching element.

Liquavista, a spin-off from Philips (www.philips.com) that has just received €12 million (about $15.5 million) in venture funding, says that it can build displays using this effect, whose fabrication will reuse much of the technology that LCD-panel construction currently employs; the active matrix, the glass substrate, and much of the production process are easily adaptable.

The company says that the display offers the only technology that can work in all modes of illumination–transmissive, transflective, or fully reflective. The company is promoting the fully reflective mode for use in handheld devices. With no backlight, a reflective-electrowetting display uses ambient light to give a bright, but low-power, display in daylight and under artificial lighting. Contrast stays constant under changing incident lighting. For color use, Liquavista says, it can build either an LCD-like RGB array or a stacked CMY (cyan-magenta-yellow)-filter structure, electronically mimicking color printing. However, first products are likely to be monochrome, TN (twisted-nematic)-type, small panels for applications such as secondary displays in cell phones. By loading the oil-dye carrier with any color, Liquavista can match the color scheme of a product or a corporate logo in the display.

The technology can switch at video speeds and support gray-scale shading, and Liquavista says it has demonstrated pixel densities of as much as 160 pixels/in.

—by Graham Prophet, *EDN Europe*

▶**Liquavista,** www.liquavista.com.

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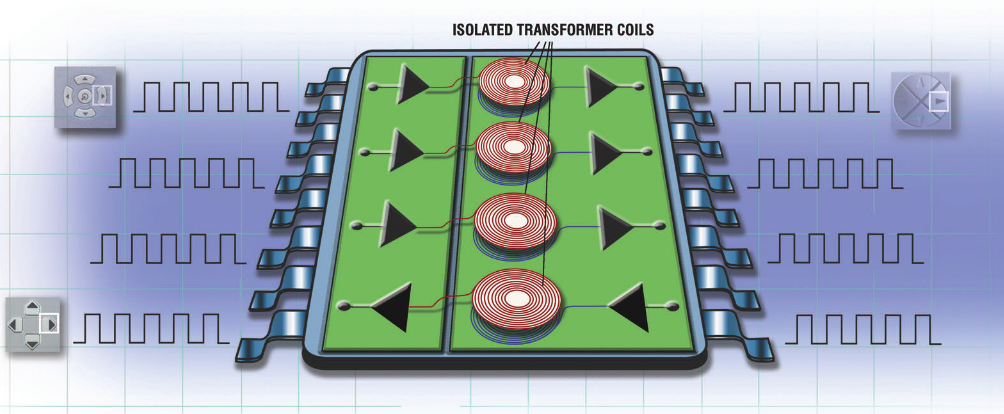

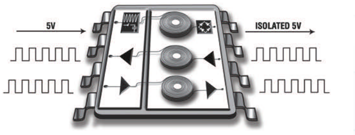

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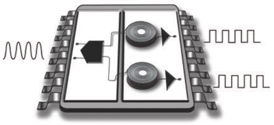

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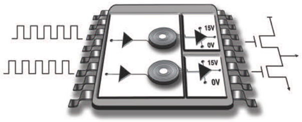

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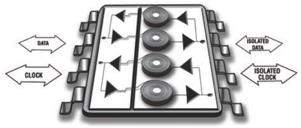

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ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Why teach science?

Jake, a high-school student, wrote to me on behalf of his science class. Our exchange follows.

Jake: What interested you in your profession?

Howard: My father is a nuclear physicist. He instilled in me a natural curiosity about how things work. In third grade, I began reading some of his old books, starting with the *Handbook of Mathematical Tables and Formulas*. At first, I couldn't understand the notation, but I understood that the book held great secrets. Later, in school, while my classmates were still adding and subtracting, I was working with square roots and complex numbers. When my dad gave me a battery and an ammeter, I became hooked on electrical engineering.

> When my dad gave me a battery and an ammeter, I became hooked on electrical engineering.

Jake: If you could talk to my classmates, what would you tell them about their education and goals?

Howard: Pick a hobby that teaches you something. Successful people absorb 99% of their knowledge outside the classroom. This idea does not mean you should skip school. It means you should learn 100 times what school has to teach. A useful hobby engages your mind and introduces you to like-minded, success-oriented people. Successful people *love to learn.*

People lacking useful skills or knowledge are forced to trade their time for money. Time is all they have to offer. An hour of uneducated time pays only about $7 in the United States.

Successful people cut a different deal with life. They do not trade their time for money. As Robert Kiyosaki outlines in his book *Rich Dad, Poor Dad*, successful people directly create value and then trade that value for money.

My way of creating value involved first learning the art of high-speed digital design. Once I mastered it, I began teaching seminars in that area. My clients pay me not for the time I spend in the classroom, but for the lifetime of experience I bring with me and for my ability to communicate that experience in a way that improves their technical capabilities and, often, changes their lives. That's value. Here's the good part: I get to sell the same lifetime of experience over and over. I've done about 250 classes so far and expect to continue for some time. That is the way value works. You never run out of it.

Jake: How does your science background help you in your everyday life?

Howard: Professional educators constantly ask this question in the hope that someone, somewhere, will articulate a convincing reason as to why all children should study science. I don't think that articulation will ever happen. Science is not for everybody. You as an individual don't really need it. You could live like an aboriginal, running around naked in the forest chasing deer with bows and arrows for all I care. There is a catch to this argument, however. The North American continent lacks the space and resources required to support hundreds of millions of low-tech, aboriginal people. Without industrial processes and machines, the vast bulk of the population would die. To avoid that catastrophe, we as a society must continually train people to build and service the machines. That is the primary purpose of science education—to seek out and find those few curious, self-motivated people who want to know how everything works and encourage them to save the rest of humanity. Quite a noble calling.

Jake: What is the most important thing you have ever learned and why?

Howard: There is no great intellectual gap separating you from the people who control the world's resources and direct its future. If any gap exists, it is only a gap of determination and will power.

Good luck to you, Jake. EDN

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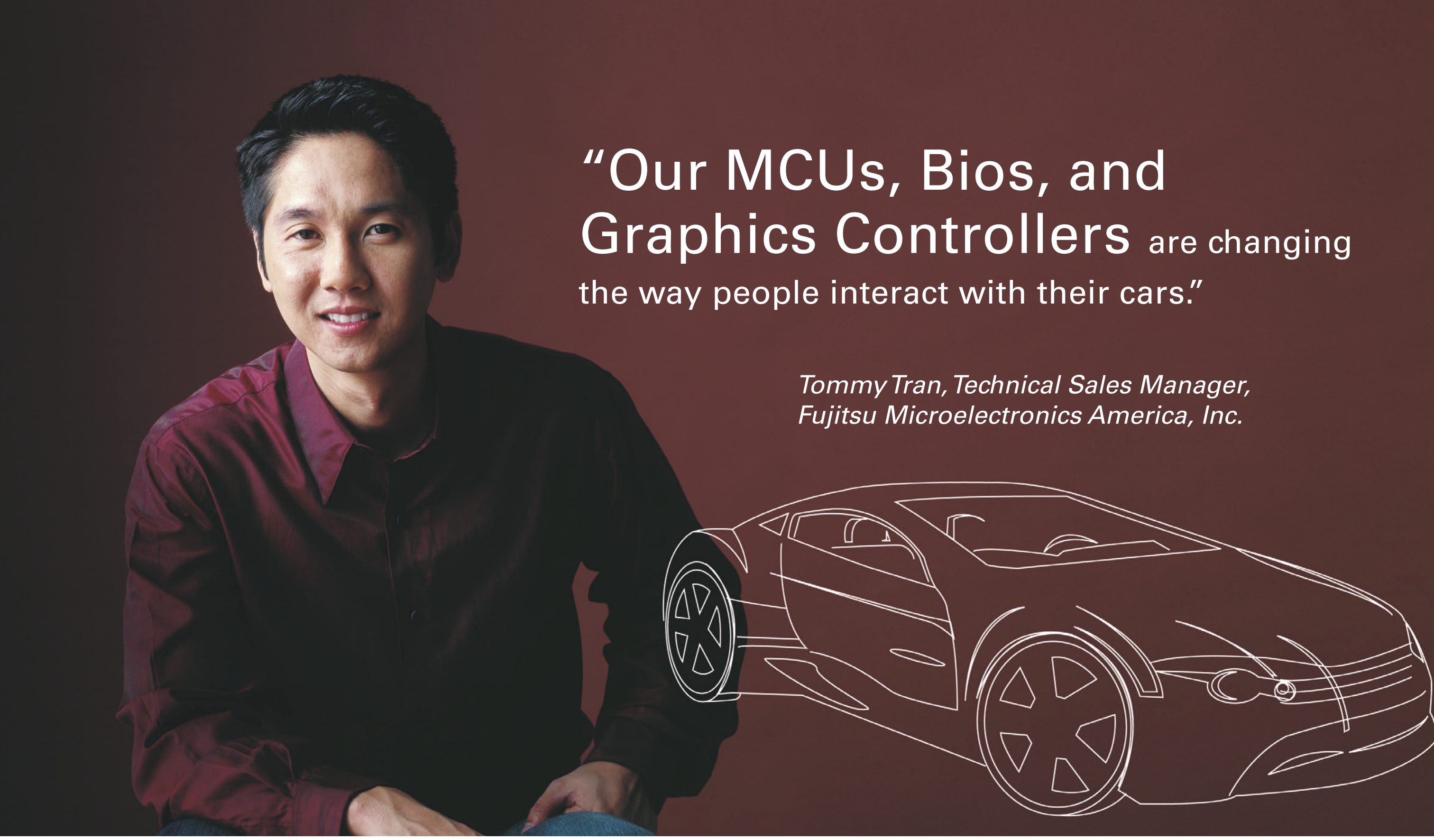
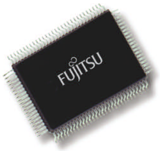
Go to www.edn.com/070201hj and click on Feedback Loop to post a comment on this column.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.





FUJITSU

TALES FROM THE CUBE

BY PAUL L SCHIMEL • FAIRCHILD SEMICONDUCTOR

You're gonna do *what* with an LCR bridge?

DANIEL VASCONCELLOS

A long time ago, when I still thought I was smart, I had just finished a transformer design and handed it off to the in-house magnetics shop. There, I learned about a technique that left me a little baffled. My drawing specified magnetizing inductance, leakage inductance, turns, phasing, pinouts, bobbin, wire, insulation systems, bake times, and the core. My expectation was that the folks in production would use a trusty old oscilloscope and a function generator to verify phase—just like I would! I was the smart one, after all.

When I checked in to see how the build was coming along, I discovered that the magnetics shop had no oscilloscope or function generator. When I asked the folks there how they measured phase, they told me that they used an LCR bridge, and the response was sharp enough to warrant my standing around for a while to see how they did it. The woman at the inspection station was mumbling something to the effect of "Looks like we gotta train the eng-HUH-neers again!" while she was jumpering pins on the bobbin.

The first test was magnetizing inductance at the primary. OK, I got that. The second test was shorting secondaries with the same primary connections. Yup, that's leakage inductance; I was still in the game. She performed similar operations for the secondary winding, most likely to check for the turns ratio looking at the ratios $\sqrt{(L_{MAG\ PRI}/L_{MAG\ SEC})}$. All right, I was still keeping up. The third test connected the secondary in series with the primary. She looked at the measurement and switched the phase on the secondary for another reading. It was a pass-fail test, no data logged. This test and its results left me puzzled. The front end of my brain was in total compression. Yet, I did have some fundamental knowledge, and I thought I knew something about flux and MMF (magnetomotive force), as I was the guy that designed the darn structure. She ran one last test to measure the dc resistance of each winding, which was reassuring in that it made sense to me. A given mean-length turn of a given wire over given turns should have consistent dc resistance. (Maybe I should have specified that fact in the drawing.) I thanked the quality-assurance woman and went back to my "eng-HUH-neering" office to ponder.

If inductance is proportional to turns squared and I have solenoidal windings around a common low reluctance path, a winding of five turns may measure an inductance of 200 μH, and another winding of 10 turns might measure an inductance of 800 μH. OK, that idea makes sense. What, then, of combinations and phase? Well, if I connect the same two windings together in series, there may be two outcomes. One outcome places the windings in phase and should yield a total of 10 plus five turns, or 1800 μH. The other outcome places the windings out of phase and yields a total of 10 minus five turns, or 200 μH. Therein lies the solution: It is possible to arbitrarily connect the windings and determine phase by flipping the polarities of one of the windings in the connection and observing the inductances associated with each phase arrangement. (Note that for this experiment to work, the windings must share the same low-reluctance flux paths.) Given this knowledge, it would also then be possible to take an arbitrary structure and determine the turns simply by unwinding a few turns and measuring the inductance before and after, or by sneaking in a few turns, again measuring the inductance before and after and noting the phase.EDN

Paul Schimel has seven years of experience as an field-applications engineer and more than six years of experience designing power supplies for consumer and industrial applications. Like Paul, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

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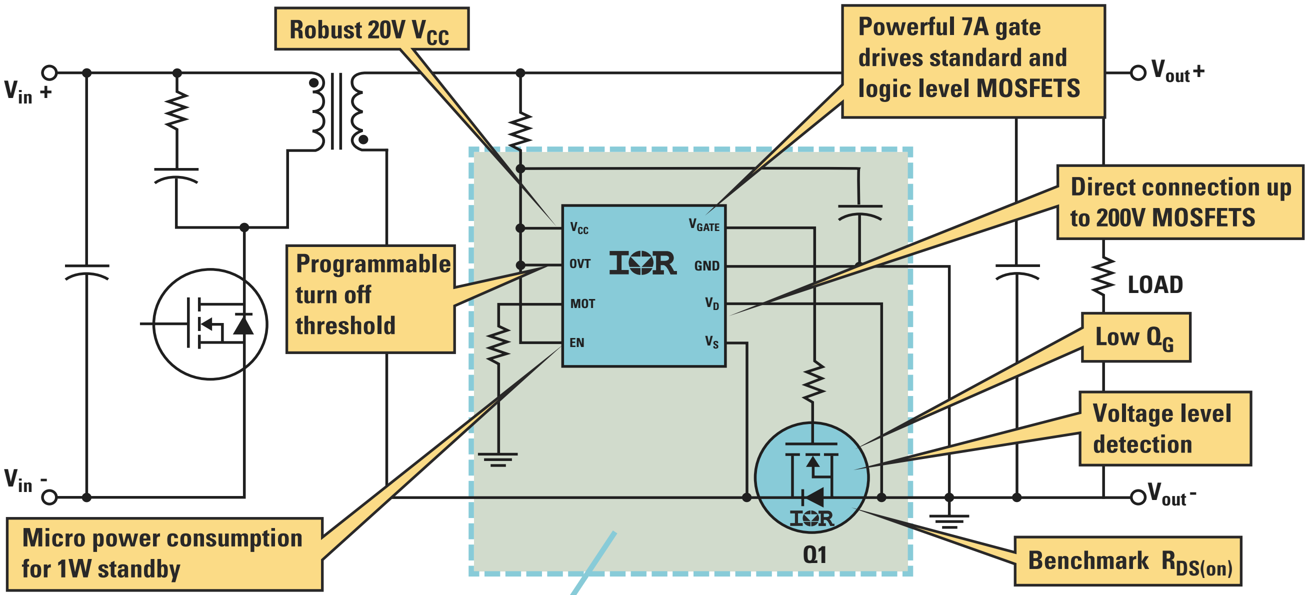

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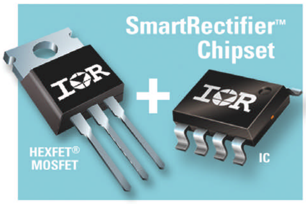

IR's new SmartRectifier™ chipset for AC-DC power converters dramatically simplifies design and improves efficiency in secondary synchronous rectification (SR) flyback and resonant half-bridge circuits, enabling a "no heatsink required" design.

Features

- Can increase system efficiency by more than 1%
- Reduces part count by up to 75%
- Works independently from primary-side control
- No current transformer required
- Industry-leading high voltage IC technology

Specifications

ICs

Part Number	Package	V_{CC} (V)	V_{FET} (V)	Sw. Freq. Max. (kHz)	Gate Drive	V_{GATE} Clamp (V)	Sleep Current Max. (µA)
IR1167A/SPbF	DIP-8/SO-8	20	<=200	500	+2A/-7A	10.7	200
IR1167B/SPbF	DIP-8/SO-8	20	<=200	500	+2A/-7A	14.5	200
IR1166/SPbF	DIP-8/SO-8	20	<=200	500	+1A/-3.5A	10.7	200

MOSFETS

Part Number	V_{DSS} (V)	$R_{DS(on)}$ max @ 10V (mΩ)	$Q_{G(typ/max)}$ (nC)	Package
IRFB3206PbF	60	3.0	120/170	TO-220
IRFB3207PbF	75	4.1	120/170	TO-220
IRF7853PbF	100	18	28/39	SO-8

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No. 116

Driving LEDs: To Cap or Not to Cap

— By Chris Richardson, Applications Engineer

Introduction

High-brightness LEDs are available today with forward currents more than 100 times greater than their predecessors. These new devices are not just high brightness, but are high power as well. Single die with dissipations of 5W and multi-die modules with power in excess of 25W are now available. The requirements of high efficiency and low dissipation dictate a switching power supply for this new generation of High-Brightness (HB), High-Power (HP) LEDs, as a voltage regulator and a current limiting resistor are no longer appropriate. High-brightness, high-power LEDs require a constant-current source to take full advantage of their ever-increasing luminous efficiency and vibrant, pure color. The topology of choice for this new breed of switching constant current sources is the basic buck converter. The most convincing argument for using a buck converter is the ease with which this simple DC-DC converter can be turned into a constant-current source. This article will explain the selection of, or possible exclusion of, an output capacitor when designing a buck regulator for constant-current drive of HB LEDs.

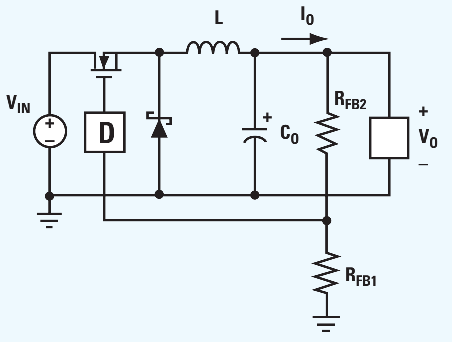


Figure 1a. Traditional Buck Voltage Regulator

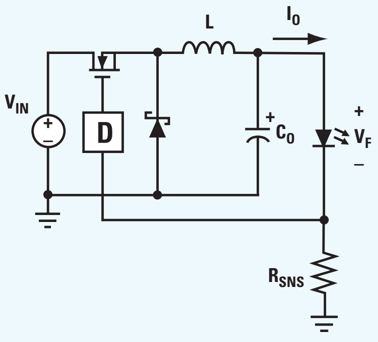


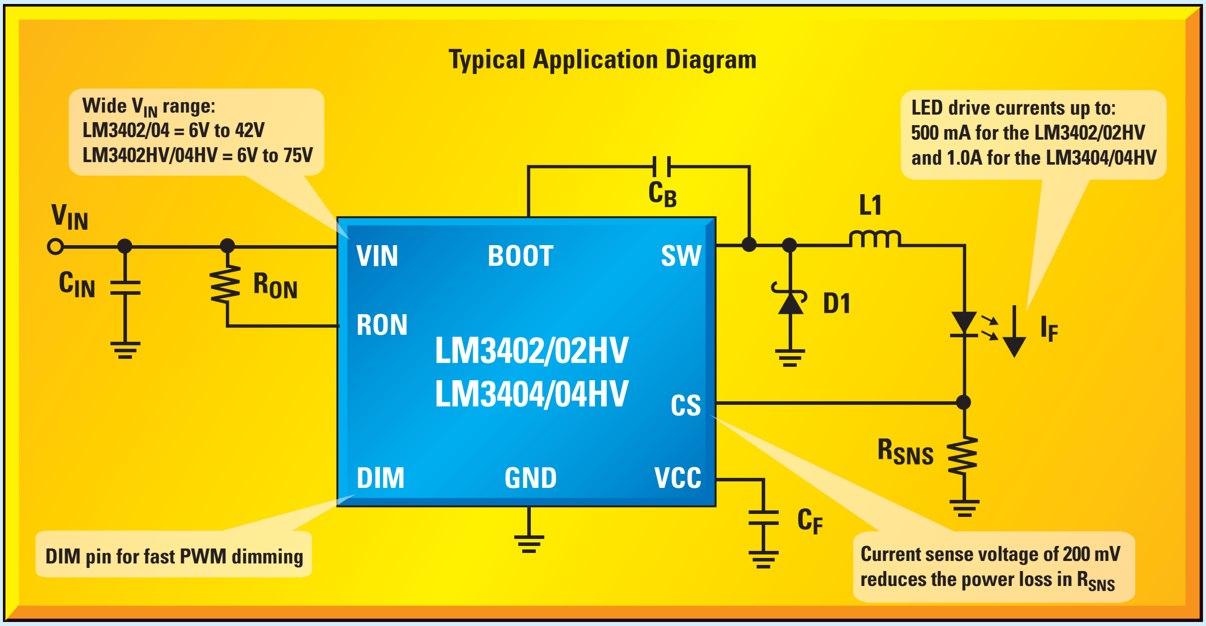
Figure 1b. Buck Current Regulator

NEXT ISSUE:
Design Challenges In Step-Down Regulator Applications

National Semiconductor
The Sight & Sound of Information

New LED Drivers Power 1W/3W LEDs up to 1A

LM3402/04 Regulators Offer Low Current-Sense Voltage to Reduce Power Loss and Deliver High Efficiency up to 95%


Typical Application Diagram

Wide V_{IN} range:
LM3402/04 = 6V to 42V
LM3402HV/04HV = 6V to 75V

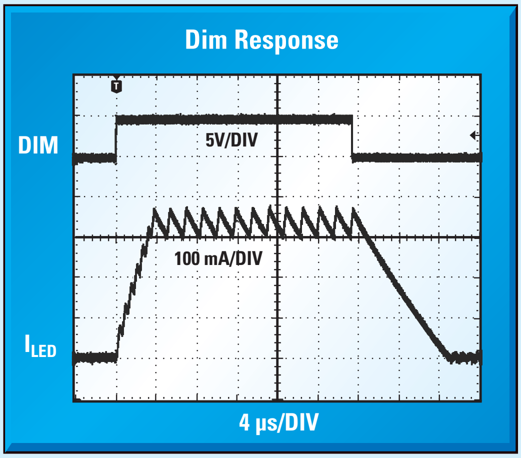
LED drive currents up to:
500 mA for the LM3402/02HV
and 1.0A for the LM3404/04HV

DIM pin for fast PWM dimming

Current sense voltage of 200 mV reduces the power loss in R_{SNS}

LM3402/04 Features

- Easy-to-use and low external parts count
- Switching frequency up to 1 MHz
- Constant on-time control with voltage feed-forward for nearly constant switching frequency over the full line voltage range
- Low 0.2V feedback reference minimizes power losses
- Low shutdown current when R_{ON} pin held low
- High voltage capability supports long strings of LEDs
- Choice of 0.5A or 1.0A peak current capability (LM3402/LM3404)


Dim Response

Ideal for use in automotive, industrial lighting, gaming/vending machines, general illumination, and architectural lighting applications

For FREE samples, datasheets, and more information, visit

www.national.com/pf/LM/LM3402.html

www.national.com/pf/LM/LM3404.html

Driving LEDs: To Cap or Not to Cap

Controlled Current

The buck regulator is uniquely suited to be a constant current driver because the output inductor is in series with the load. Regardless of whether a buck regulator is used as a voltage source or a current source, selection of the inductor forms the cornerstone of the system design. With an inductor in series with the output, the average inductor current is always equal to the average output current, and the buck converter naturally maintains control of the AC-current ripple. By definition, the LED drive is a constant load system; hence a large amount of output capacitance is not necessary to maintain V_O during load transients.

No Output Cap Yields High Output Impedance

In theory, a perfect current source has infinite output impedance, allowing the voltage to slew infinitely fast in order to maintain a constant current. For switching regulator designers who have concentrated on voltage regulators, this concept may take a moment to sink in. Completely removing the output capacitor from a buck regulator forces the output impedance to depend on the inductor. Without any capacitance to oppose changes in V_O, the output current (referred to as forward current, or I_F) slew rate depends entirely upon the inductance, the input voltage, and the output voltage. (V_O is equal to the combined forward voltage, V_F, of each series-connected LED)

LED manufacturers generally recommend a ripple current, ΔI_F, of ±5% to ±20% of the DC forward current. Over the typical switching regulator frequency range of 50 kHz to 2 MHz the ripple itself is not visible to the human eye. These limits come from increasing thermal losses at higher ripple current (a property of the LED semiconductor PN junction itself) and a practical limit to the inductance used. The percentages are similar to the recommended current ripple ratio in buck voltage regulators. Inductor selection for a fixed-frequency current regulator is therefore governed by the same equations as a voltage regulator:

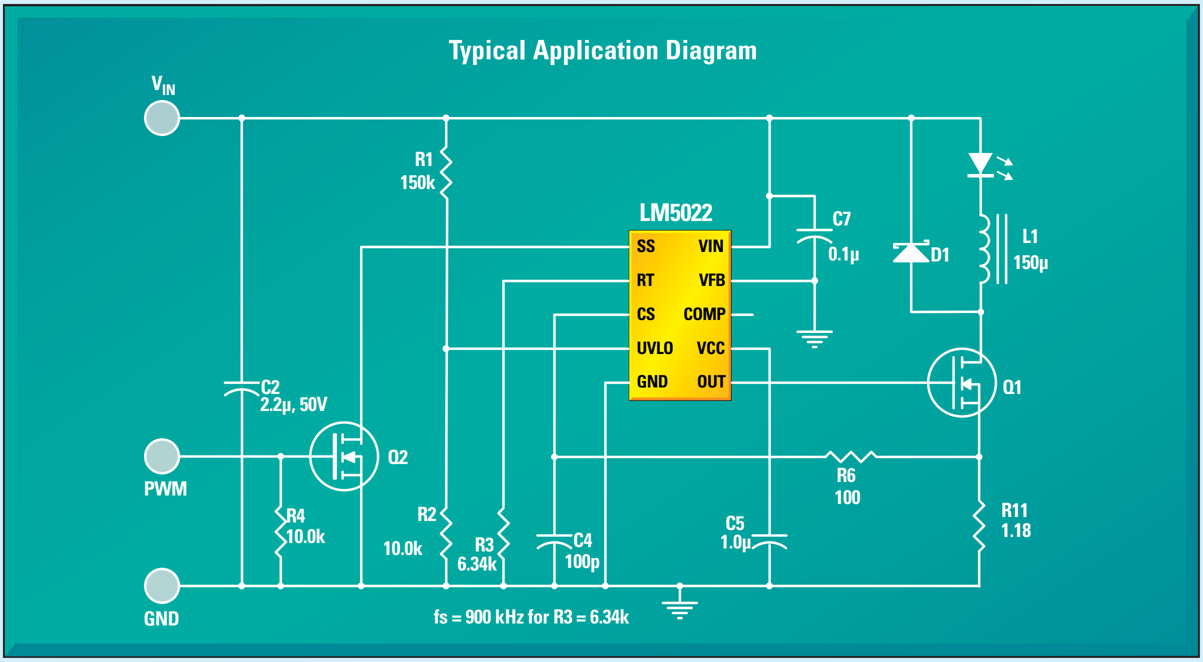
$$L = \frac{V_{IN}}{V_F} \times \frac{V_{IN} - V_F}{\Delta i_L \times f_{SW}}$$

One difference is that the inductance used for current regulators without output capacitors tends to be higher because the drive currents for the emerging standards of 1W, 3W, and 5W HB LEDs are 350 mA, 700 mA, and 1A respectively. Modern buck voltage regulators tend to use inductors in the range of 0.1 µH to 10 µH with saturation currents from 5A to 50A. Current drivers at similar switching frequencies tend to require inductors ranging from 10 µH to 1000 µH and saturation currents ranging from 0.5A to 5A.

The main goal of high output impedance is to create a system capable of responding to PWM dimming signals, the preferred method of controlling the light output of LEDs. The dimming signal might be applied to the enable pin of the regulator, in which case the output current can slew from zero to the target and back to zero without the delay of C_O being charged and discharged. For even faster, higher resolution dimming, a shunt switch, usually a MOSFET, can be placed in parallel with the LED array, allowing the continuous flow of current at all times. Again, with no output capacitor to slow the slew rate, dimming frequencies into the 10's of kHz are possible. This is a critical requirement in applications such as backlighting of flat-panel displays, and the creation of white light using an RGB array.

High Voltage Current Mode Controller with Ultra-Wide Input Voltage Range

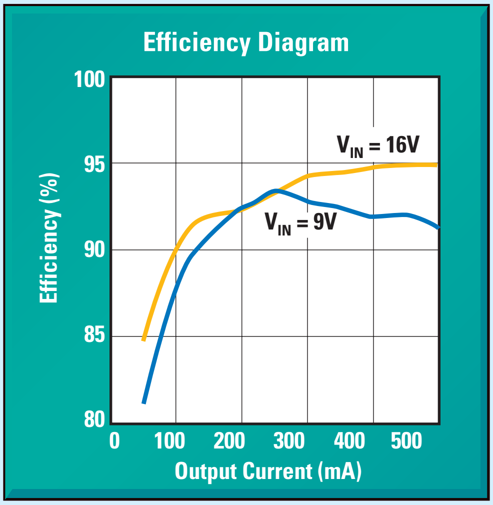
LM5022 with 6V to 60V Input Capability Controls an External MOSFET to Deliver Higher Current to LEDs


Typical Application Diagram

fs = 900 kHz for R3 = 6.34k

LM5022 Features

- Internal 60V startup regulator
- 1A peak N-Channel MOSFET gate driver
- V_{IN} range 6V to 60V
- Duty cycle limit in excess of 90%
- Programmable UVLO with hysteresis
- Cycle-by-cycle current limit
- Single resistor oscillator frequency set
- Slope compensation
- Adjustable soft-start
- Available in MSOP-10 packaging


Efficiency Diagram

Ideal for use in boost and SEPIC converters for automotive and industrial applications, and for ground-referenced applications such as forward and flyback regulators

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Driving LEDs: To Cap or Not to Cap

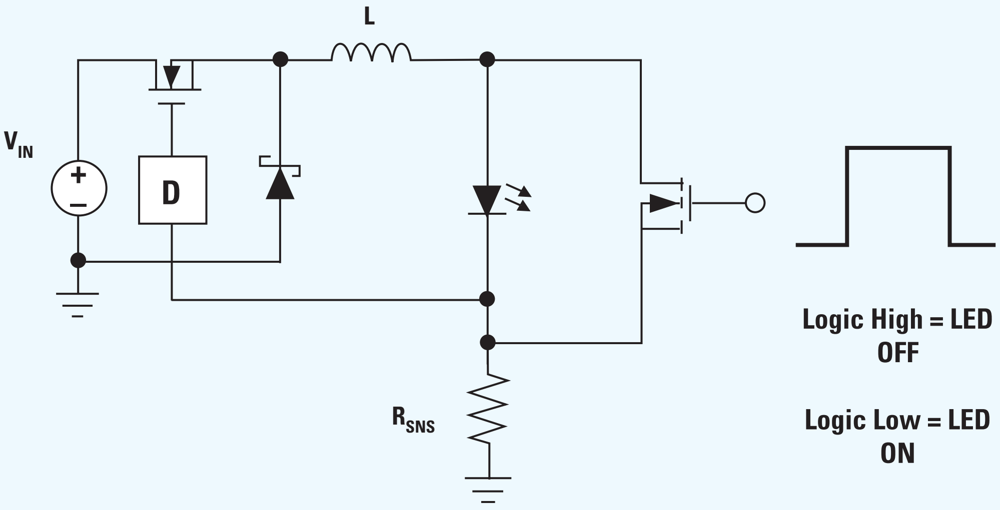

Figure 2. Dimming with a Parallel NFET

Using an Output Capacitor Reduces Size and Cost

Some amount of output capacitance can be useful as an AC current filter. Applications such as retro-fitting of incandescent and halogen lights often require that the LED and driver be placed in a small space formerly occupied by a light bulb. Invariably the inductor is the largest, most expensive component after the LEDs themselves. For the sake of efficiency (especially important in cramped quarters), the designer generally chooses the lowest switching frequency that allows the solution (mostly the inductor) to fit. Allowing a large ripple current in the inductor and filtering the LED current results in a smaller, less expensive solution. For example, to drive a single white LED ($V_F \approx 3.5V$) at 1A with a ripple current Δi_F of ±5% from an input of 12V at 500 kHz would require a 50 µH inductor with a current rating of 1.1A. A typical ferrite core device that fits this application might be 10 mm square and 4.5 mm in height. In contrast, if the inductor ripple current is allowed to increase to ±30% (typical for a low-current voltage regulator) then the inductance required is less than 10 µH, and an inductor measuring 6.0 mm square and only 2.8 mm in height size can be used. The output capacitance required is calculated based on the dynamic resistance, r_D, of the LED, the sense resistance, R_{SNS}, and the impedance of the capacitor at the switching frequency, using the following expressions:

$$C_O = \frac{1}{2\pi \times f_{SW} \times (ESR + Z_C)}, \quad Z_C = \frac{\Delta i_F}{\Delta i_L - \Delta i_F} \times r_D$$

Typical values for output capacitors range from 0.1 µF to 10 µF, a perfect fit for ceramic capacitors. In many applications, the addition of an output capacitor reduces both the size and the cost of the total solution.

Output Capacitor Placement

For buck regulators that use PWM-based control, such as Voltage Mode (VM) and Current Mode (CM) the output capacitor should be connected from the regulator output to system ground,

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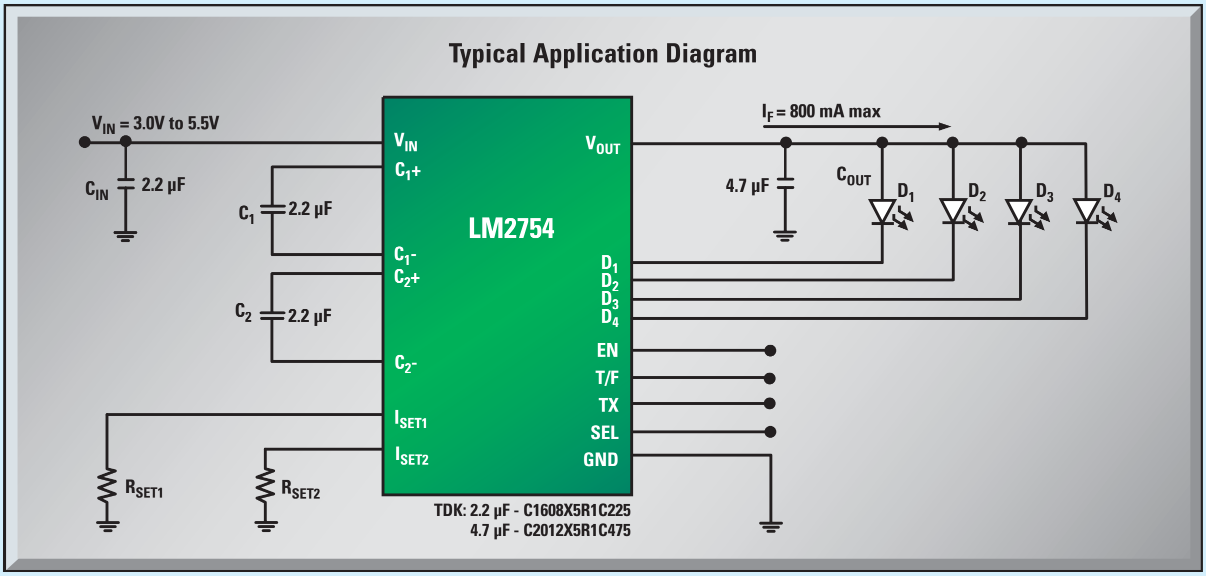
Typical Application Diagram

TDK: 2.2 µF - C1608X5R1C225
4.7 µF - C2012X5R1C475

LM2754 Features

- Total solution size without LED < 28 mm^2
- Time-out circuit limit flash duration to 1s, protects LED from over-heating
- No inductor required
- True shutdown output disconnect
- <1 µA shutdown current
- TX input ensures synchronization with RF power amplifier pulse
- Ability to disable one current sink via the SEL pin to accommodate 3-LED flash modules
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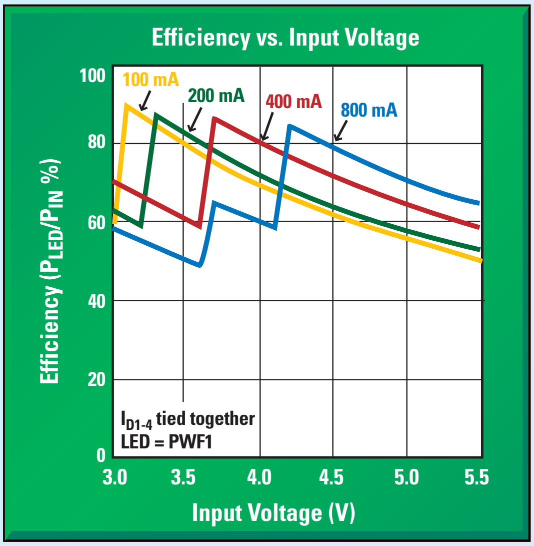
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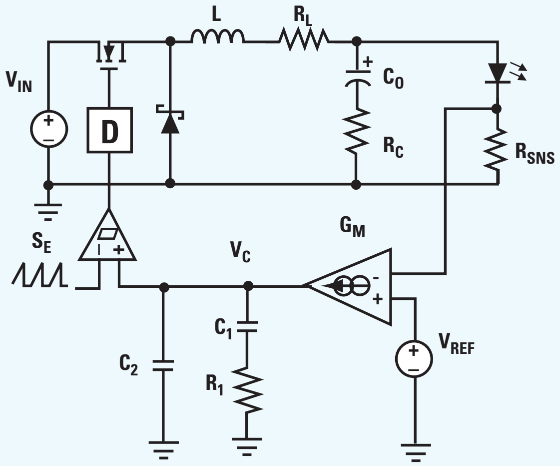


Figure 3a: PWM Regulator

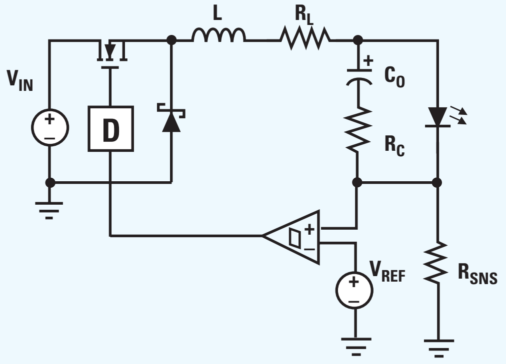


Figure 3b: Comparator-based Regulator

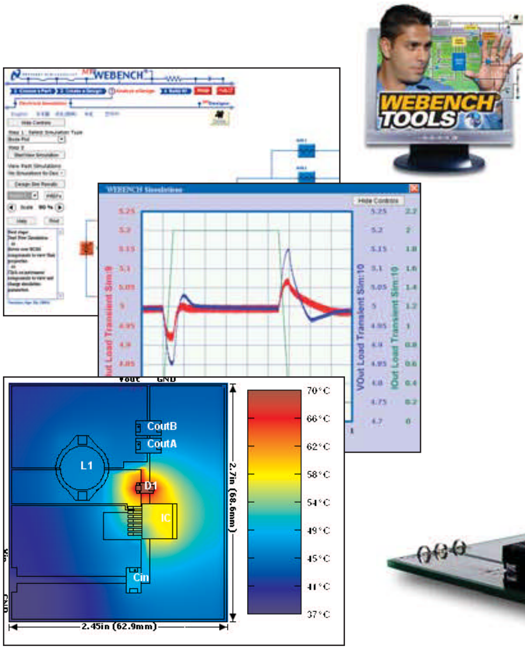
identical to a normal buck regulator. *(Figure 3a)* This way, the control-to-output transfer function of the system can be analyzed with the same equations used when designing a voltage regulator. When using comparator-based control, such as hysteretic or Constant on-Time (COT), the output capacitor should be placed in parallel with the LED array. *(Figure 3b)* In hysteretic voltage regulator circuits, this technique is often used to increase the percentage of in-phase voltage ripple at the feedback node. For the current regulator, it forces both the ripple current through C_O and the forward current through the LEDs to sum at the input to the switching comparator. The voltage waveform across R_{SNS} is therefore in-phase with the switching node waveform, and the result is predictable operation with high noise rejection. The combination of low output capacitance and high inductor current ripple actually makes hysteretic and COT current regulators more reliable and easier to design than voltage regulators.

Conclusion

The high brightness, high power LED represents the biggest change in lighting design since the introduction of fluorescent bulbs. Using LEDs requires a fundamental change in the complexity of electronics used for lighting systems. Currently a large portion of LED lighting design is retrofitting of incandescent, halogen, and fluorescent installations. Such systems rarely include sophisticated dimming control, and place a high value on small size. These are the applications where an output capacitor is a welcome addition to the driver circuit.

In the future, the higher cost of LEDs for general lighting will be balanced by new levels of control over brightness, tone, and color. Lighting in homes and businesses will require fast PWM dimming, requiring current drivers to minimize or eliminate their output capacitance. These systems will draw upon experience from today's fast-dimming applications which have already shed the output capacitor to provide the best response time. ■

Power Design Tools



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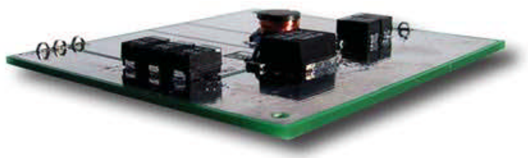

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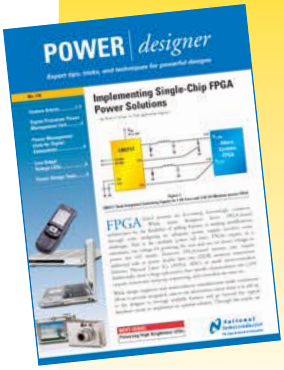

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INNOVATOR OF THE YEAR FINALISTS

iMotion team (Toshio Takahashi, Eddy Ho, Seok Joon Hong, Ilia Greenblat, Sergio Morini, Fabio Necco), International Rectifier

Although the washing machine is not the most exciting product in today's digital home, it represents a huge challenge to designers at white-goods manufacturers. The presence of water and heat makes for a harsh environment, and both government agencies and consumers mandate the need to reduce power. The International Rectifier design team behind the mixed-signal iMotion IRMCF341 motor-control IC directly attacked the challenges of reliability, low power, quiet operation, and size and simplified the process for the design engineer.

Project Director Toshio Takahashi and iMotion-team members Ilia Greenblat, Eddy Ho, Seok Joon Hong, Sergio Morini, and Fabio Necco led a mixed-discipline design and tapped engineers spread from North America throughout Europe and into Israel. The team used a signal-processor approach yet with algorithms implemented in configurable hardware. The result is a controller for permanent-magnet motors that features sensorless speed control by means of dc-link current measurements.

International Rectifier claims that the design reduces motor and drive costs by 30% over competing controllers. Perhaps more important for consumers is the company's claim that the design can slash energy use by 70%.

Virtex-5 LXT FPGA design team (Steve Douglass, Suresh Menon, and team), Xilinx

A lot of product designs face a roadblock, but few face the number of obstacles that Steve Douglass, Suresh Menon, and their Virtex-5 LXT design team did. The FPGA design included a move to a 65-nm process, necessitated a balance of programmability and hard-IP (intellectual-property) features, and realistically required a solution to ballooning dynamic-power consumption. The result is a chip that has more than a billion transistors, yet, according to Xilinx, it uses 35% less dynamic power than earlier 90-nm designs.

The Virtex-5 LXT team included more than 200 engineers organized into groups called Centers of Excellence, with each group focusing on an aspect of the new architecture. Product planners met with hundreds of system designers to get input on the new architecture. The company claims that the result is 30% higher performance and 65% higher logic density.

The Virtex-5 LXT design leads a trend of balanced programmability and fixed functions. The chip includes built-in hard-IP blocks for what Xilinx claims are the two most popular serial-I/O standards: PCIe (PCI Express) and Gigabit Ethernet.

Kenneth Parker, senior scientist, Agilent

Everyone likes to get something for nothing. Essentially, that's what Kenneth Parker and his Medalist bead-probe team at Agilent are promising to engineers that must design boards that they can test using ICT (in-circuit-testing) techniques. With higher speed circuits and denser boards, traditional ICT techniques are out of gas and could lead to more expensive and less effective testing of complex boards. Agilent claims that the Medalist bead-probe approach preserves the use of ICT, at minimal costs.

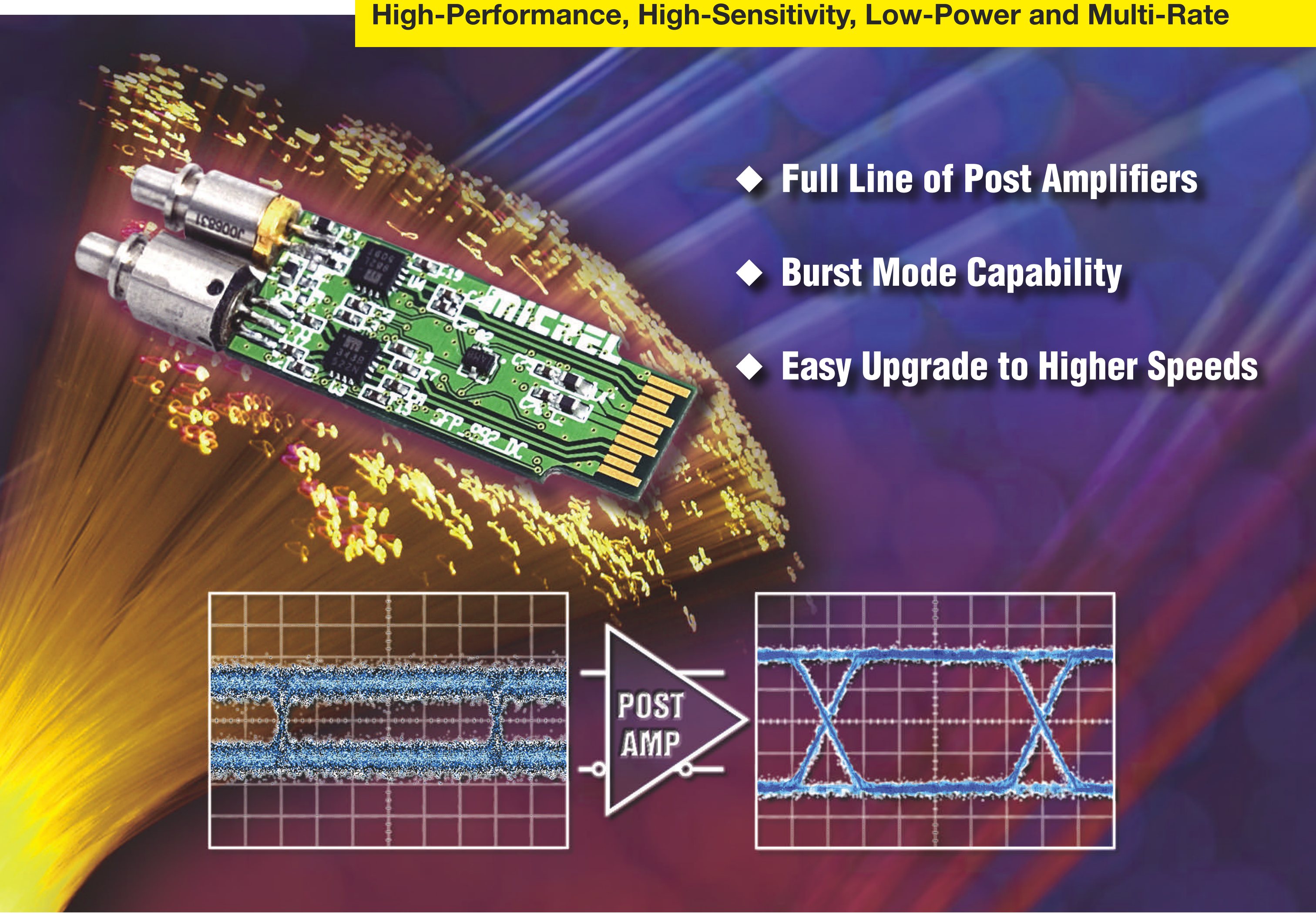
Agilent's bead-probe technology places test targets directly on pc-board signal traces. The beads then serve as highly reliable test points for use during ICT. Agilent claims that the new technique dramatically improves ICT access on high-density and -speed boards, resulting in excellent fault coverage. Surface-mount production lines can support the technology. The reflow solder process creates the bead probes in any spots left open in the design of the solder mask.

Dr Kaigham (Ken) J Gabriel, Akustica

It may seem strange, at first glance, to encounter a microphone as an *EDN* Innovation Award candidate. After all, the materials that constitute ECMs (electret-condenser microphones) have existed since the 1920s, and Bell Laboratories unveiled the first practical ECM, based on thin metallized Teflon foil, in 1962. MEMS (microelectrical-mechanical systems), however, have fundamentally changed the way microphones work, and Akustica has pushed that trend, adding circuitry in the AKU2000 digital microphone that can produce a digital output. Moreover, Akustica claims its techniques rely on a pure CMOS process that could yield many other types of smart sensors.

Akustica Co-Founder, Chairman, and Chief Technology Officer Ken Gabriel led the development based on what the company calls CMOS MEMS. The CMOS MEMS process builds MEMS structures directly inside CMOS materials. The company claims that it fabricates the structures from the metal-dielectric layers of the CMOS, which are deposited during the standard CMOS-processing flow. Other MEMS technologies, which are fabricated in films on top of CMOS, don't offer the ability to integrate sensors and analog and digital circuits on a monolithic IC.

Akustica claims that it can produce microphones with better than four times the uniformity of ECMs.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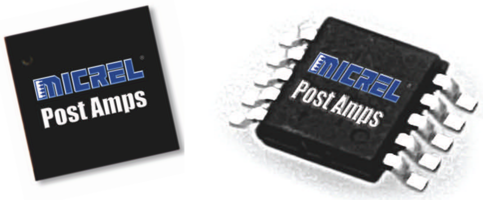
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Hazardous-voltage primer by David Lohbeck, National Instruments, May 11, 2006, www.edn.com/article/CA6330100

Magnetic-field measurements hold the key to reducing dc/dc EMI by William J Bowhers, Merrimack College, July 20, 2006, www.edn.com/article/CA6351292

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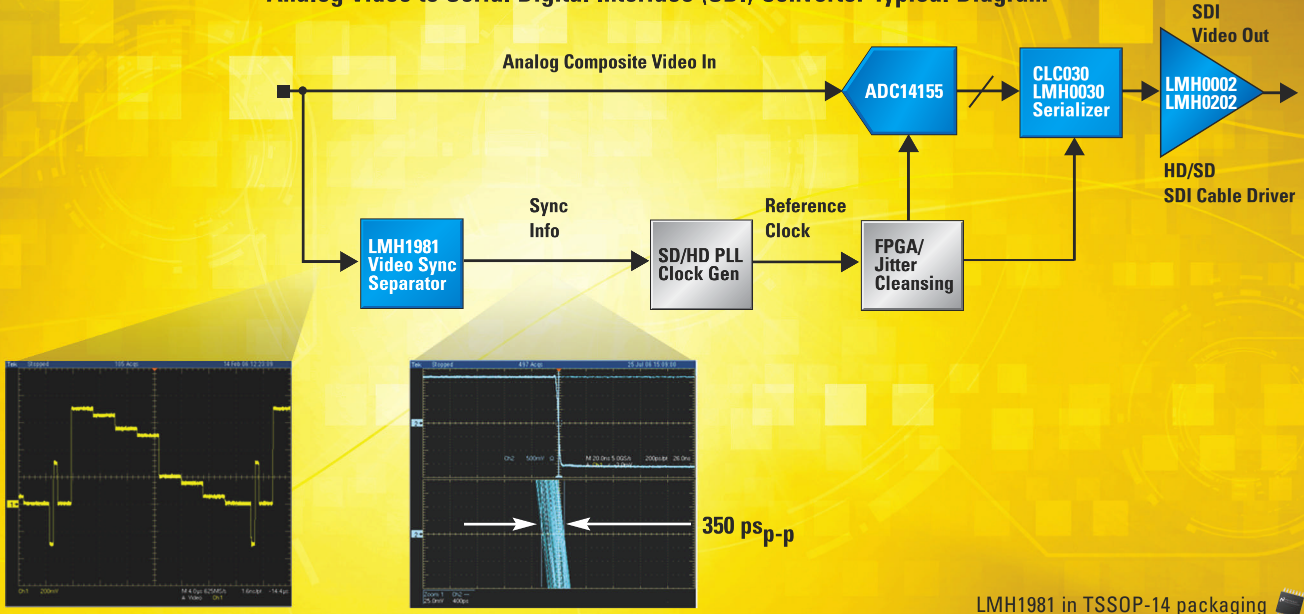

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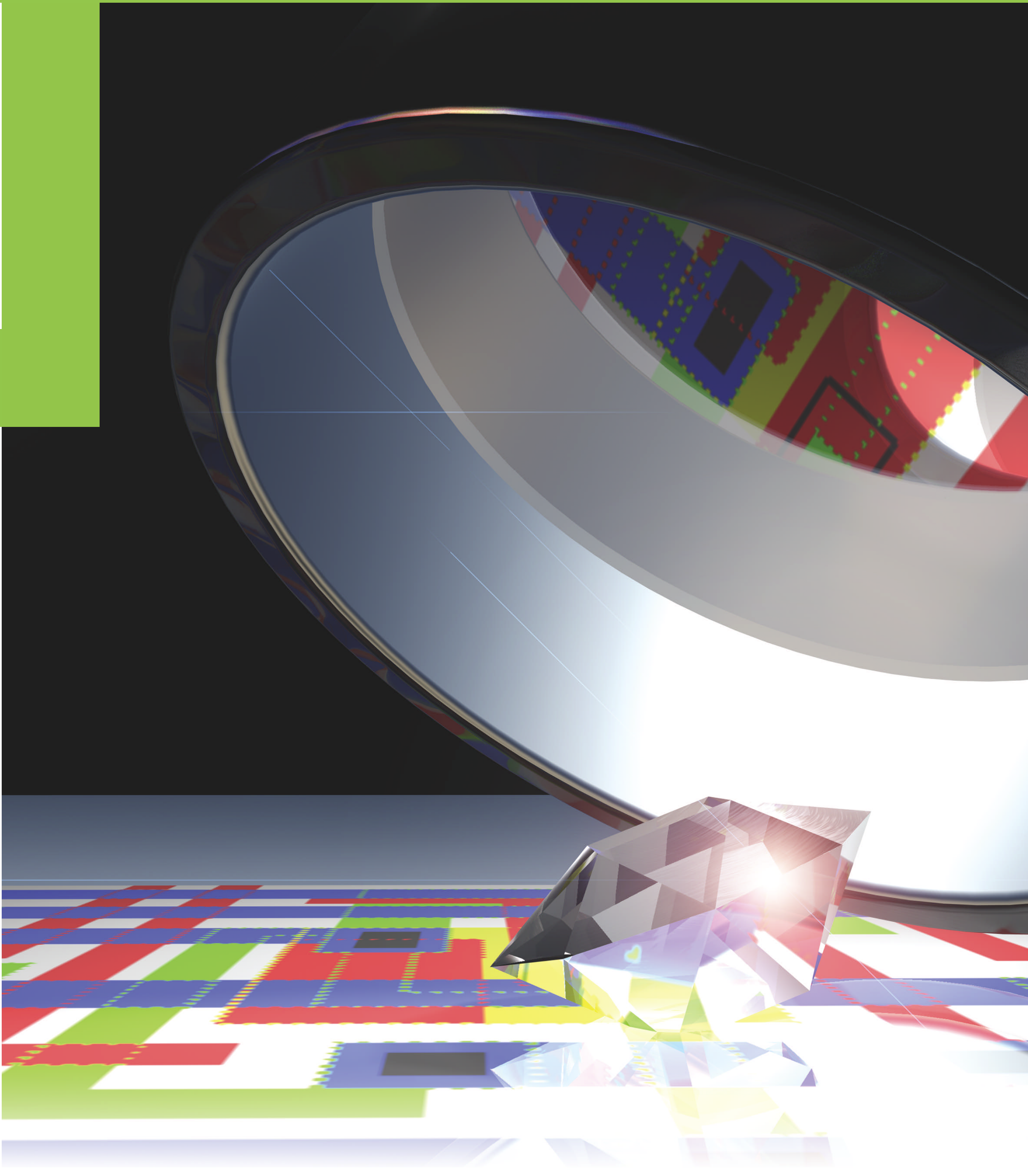
BY MICHAEL SANTARINI • SENIOR EDITOR

Evaluating IP with the four Cs: COMPARE CONSIDER COLLECT CALCULATE

FINDING QUALITY IP IS ONE OF THE BIGGEST HEADACHES IN IC DESIGN. FORTUNATELY, THERE ARE A FEW RESOURCES AS WELL AS TIPS AND TRICKS TO HELP DESIGNERS HOME IN ON THE BEST CHOICE. CONSIDER THE FOUR Cs: COMPARE MANY CORES, CONSIDER VENDOR SIZE, COLLECT REFERENCES, AND CALCULATE RISKS.

There wasn't a big ceremony with fireworks, a comedian, and showgirls in stunning dresses. There was no party, and there wasn't even a press release, but, last year, the IP (intellectual-property) industry quietly celebrated its 10th anniversary. Its debut coincided with the 1996 formation of the VSIA (Virtual Socket Initiative Alliance). You might find that fact hard to believe given that it is now nearly impossible to find an SOC (system on chip) or an ASIC that does not contain at least one reused block—that is, one piece of IP. But the unceremonious passing of the IP industry's 10th anniversary is a testament to the fact that the industry has a long way to go before reaching its full potential.

In 1995, new IC-process nodes of 0.35 and 0.25 micron presented the IC-design community with a huge problem: How would designers be able to use all the gates that new "deep submicron" made available? To its credit, the IC-design community mobilized quickly and converged on a single idea: The way to fill up these huge, 100,000-gate designs was to reuse large blocks from previous designs or to purchase blocks from vendors. The main idea was that design groups would implement the reused or acquired blocks in their new designs, add their own value-added logic blocks to their designs, and then simply connect all those blocks with a bit of glue logic. It sounds easy! Within a year, hundreds of design houses, big EDA vendors, and under-the-radar IP vendors—such as ARM, which had been



offering microprocessor cores since the mid-1980s—all started flaunting IP offerings and formed the beginning of what we today call the IP industry.

Although designing with reused blocks sounded great in theory, however, the technical details and implementation were less simple in practice, as well as in the legal issues the reusable IP brought up. So, the IP industry in its infancy defined two key technical objectives it needed to make IP-based design a success: Create a single standard bus that would allow IP blocks from disparate vendors to communicate—that is, plug and play—and establish a standard—ISO 9000—that would ensure that various blocks from different vendors achieved a certain quality. The thinking was: If the cores conformed to a standard, designers could more easily connect the cores to the standard bus and vastly speed the design of ICs.

To establish these standards and work on other IP-related technical issues, the semiconductor, EDA, and IP vendors banded together to form the VSIA, which they launched in 1996 with 35 member companies. When they first launched it, it seemed as if every vendor in the design community wanted to join the effort to have some influence on or at least be in the know about VSIA's development of standards, so that, when the VSIA released a standard, member companies could quickly adopt it and crank out new, innovative products based upon it.

AT A GLANCE

- The formation of the VSIA (Virtual Socket Initiative Alliance) in 1996 marked the beginning of the IP (intellectual-property) industry.
- Gartner expects the IP industry to post revenue of $1.8 billion for 2006.
- IP quality remains a top concern for IC designers.
- Groups such as VSIA and, more recently, the FSA (Fabless Semiconductor Association) are tackling quality problems.

One of the VSIA's first tasks was to form a standard, common on-chip bus. Seemingly, every VSIA member company wanted to influence the bus or bus protocol, so, trying to be diplomatic, the VSIA's OCB DWG (On-Chip Bus Development Working Group) paid special attention to making the OCB all-inclusive and to serving multiple application areas. The DWG took several years to finally deliver the OCB to the community. But, while the OCB DWG was producing OCB, vendors such as ARM and Sonics, along with several semiconductor companies, quickly developed their own buses. When VSIA finally did unveil its OCB, the industry considered the bus too general and too inefficient for use in most IC designs. Few adopted it, the effort died, and the remains went to OCP IP (On-Chip Protocol International Partnership). Fortunately, the industry did rally around application-specific buses from Sonics and ARM with its AMBA (Advanced Microcontroller Bus Architecture) and several proprietary buses from ASIC houses and IDMs (integrated-device manufacturers). Designers still use those buses today, and choosing one over the other largely depends on the targeted application or IC manufacturer.

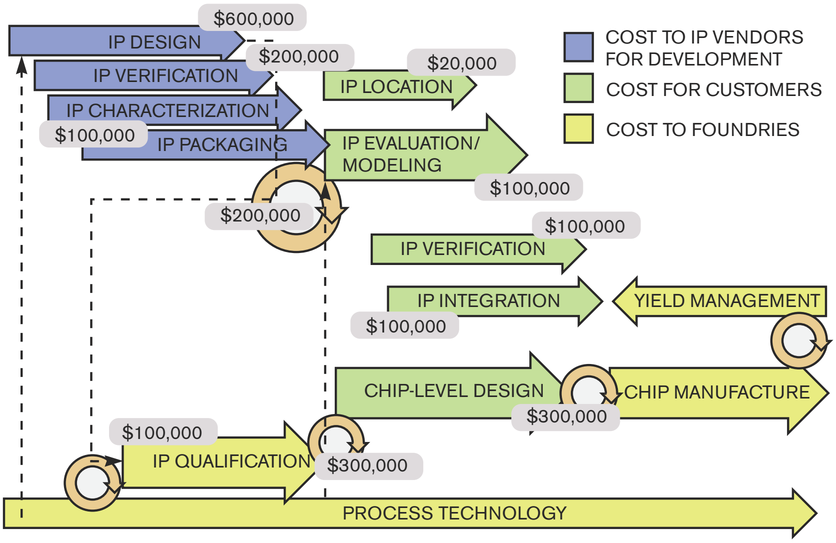


Figure 1 The cost of IP goes beyond the IP license. In this example, the IP costs explicitly $900,000 to develop, but the total ecosystem cost is $2.02 million (courtesy Fabless Semiconductor Association).

However, choosing to go with several application-specific buses rather than a single bus, the industry further complicated the formation of a quality standard. In the late '90s, Synopsys, which had developed its own portfolio of IP, developed the "Open More" quality metric, a check list for IP-vendor cores that ultimately assigned a single "grade" for each piece of IP based on a given core's conformance to the check list criteria. Synopsys first used this check list for its own IP development, but, seeing that it could have greater use for the industry and knowing that Synopsys IP already scored high according to the metric, Synopsys donated it to the VSIA, which renamed it the QIP (quality-IP) metric. The main hope for QIP was that all IP vendors and IC companies creating their own large IP repositories would adopt the QIP and that the VSIA would maintain a master list of the world's IP that would allow customers to quickly find the highest ranked cores.

Today, the industry widely acknowledges the QIP metric as a useful way to measure IP conformance to certain quality guidelines. Many customers now ask IP vendors to provide a QIP score with their IP. VSIA claims that the QIP effort is going strong (see **sidebar** "VSIA's QIP making strides"). But overwhelming participation is so far lacking from the IP or vendor communities in submitting their cores to a single common resource or repository that would allow users to do side-by-side comparisons of similar types of IP.

The master list hasn't come to fruition for several reasons. For one thing, multiple buses and applications dictate the need for flexible or multiple qual-

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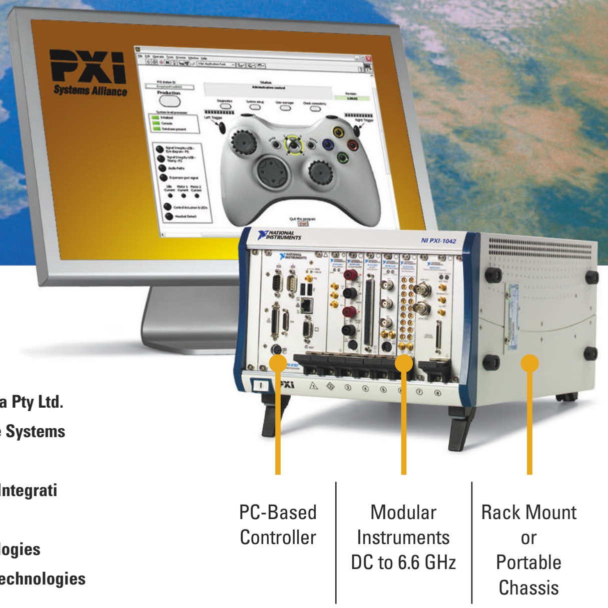

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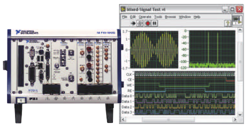

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ity standards. Further, political issues and lingering feelings from VSIA's failure to deliver a viable OCB soured folks from participating in subsequent VSIA efforts. Also, there is a lack of unity among IP vendors. In retrospect, that idea of a master list may have been too ambitious in the first place. But if you ask designers today what is the single biggest issue with IP, the answer is almost always "IP quality."

TABLE 1 SAMPLE OF FSA'S HIP QUESTIONS

Categories	Questions
IP design	Does the IP include a test-pan document?
IP verification	Does the IP come with a comprehensive verification environment?
IP design	Does the IP contain analog circuitry or high-speed custom digital?
IP design	Are the device-model-date codes and revision information documented?
Process technology	Has the foundry released more up-to-date device models than were used when this IP was designed?
Reliability	Does the IP contain memory?
Verification	Does the IP include a portion that is delivered soft as RTL?

"It's really as bad as you would think," says Richard Tobias, former chief technology officer at Pixelworks. "The 'star' IP vendors, such as ARM and MIPS, do a pretty good job of presenting quality IP, but the smaller, independent vendors don't typically do as well, and you have to do some extra work. If it's analog IP, you always have to do a lot of extra work."

Norbert Diesing, director of technology access at PMC-Sierra, agrees. "You trust some IP vendors more than others," he said at a fall 2006 FSA (Fabless Semiconductor Association) panel. "But there's always some degree of mistrust. In our experience, the quality of the IP deliverables is lacking, and, in most cases, the IP vendor hasn't done enough verification of its own IP." Diesing said that PMC-Sierra has run into trouble in the past with overrunning IP-design budgets, so the company's design managers now regularly tack on an additional 30% over the IP-licensing costs to cover the additional costs of getting the IP to work in their design. Much of that expense goes toward reverifying the functions of a hard core and ensuring that it works with a given foundry's process technology. Other designers note that, if a given core is standards-based, as are the PCI (Peripheral Component Interconnect) and PCIe (PCI Express) communication cores, designers also must reverify that the core complies with the standard's protocol.

Low-quality IP can create extra expenses not only for customers, but also for foundries and, in turn, IP vendors. FSA officials believe that a poor core can create additional expenses across the whole IC-design ecosystem (**Figure 1**). Low-quality IP leads to extra costs, and this problem has become so big that, at the urging of its member companies, FSA in late 2003 collaborated with the VSIA to help invigorate and speed the VSIA's development of the QIP. "The small fabless vendors are perhaps the most uneducated when it comes to their IP-buying practices," said Jim Ensell, senior vice president of marketing and business development at Virage Logic, during the fall 2006 FSA panel. "Those folks tend to buy IP believing it is going to work the first time; they don't initially account for all the cost it is going to take to rework the IP." FSA did help to further QIP-metric development. VSIA has recently extended QIP to simulation models, or verification IP. However, last year, FSA split from the VSIA to create the HIP (hard-IP)-quality-risk-assessment tool.

Raminderpal Singh, senior engineering manager at IBM Microelectronics, headed the development of the FSA tool. He says that the tool, free for downloading from the FSA's Web site, seeks to help companies compare IP and evaluate the risks and subsequent costs of selecting a vendor's IP. Whereas the QIP has a standard set of questions for all cores, assigns a single score to a piece of IP, and mainly focuses on soft and verification IP, the HIP scores IP in seven

VSIA'S QIP MAKING STRIDES

In its 11th year, the VSIA (Virtual Socket Initiative Alliance) and its QIP (quality-intellectual-property) metric are alive and well, says VSIA President Kathy Werner. VSIA has more than 40 member companies, a list of which you can see at http://vsi.org/members/index.htm. The organization's QIP metric has been publicly available since January 2006, and visitors to the Web site have downloaded it more than 1000 times.

"The VSIA QIP metric really helps compare apples to apples," says Werner. "If I am looking at purchasing a similar core, I want to know a number of things, including what information is available, which company has had successful tapeout, what level of technical support it includes, and what fits best with my design implementation and methodologies. Having this information enables a designer to mitigate their risk when purchasing a core to integrate into their design."

Werner says the VSIA is also working with the CSIA (China Semiconductor Industry Association) to make QIP the official standard-quality metric for China and to enhance the QIP metric with a deliverables check list. Researchers from the Hong Kong University of Science and Technology, along with researchers from three mainland China universities, developed the deliverables check list, basing it on VSIA deliverables from QIP line items.

The QIP metric is available for free downloading from the VSIA Web site. However, a company must join the VSIA if it wants to influence new worksheets, including the verification spreadsheet, or the update to the hard-IP spreadsheet. Once the new spreadsheets have gone through beta testing, VSIA will make them freely available to the public. Users can download the QIP at http://www.vsia.org/qipdownload/.

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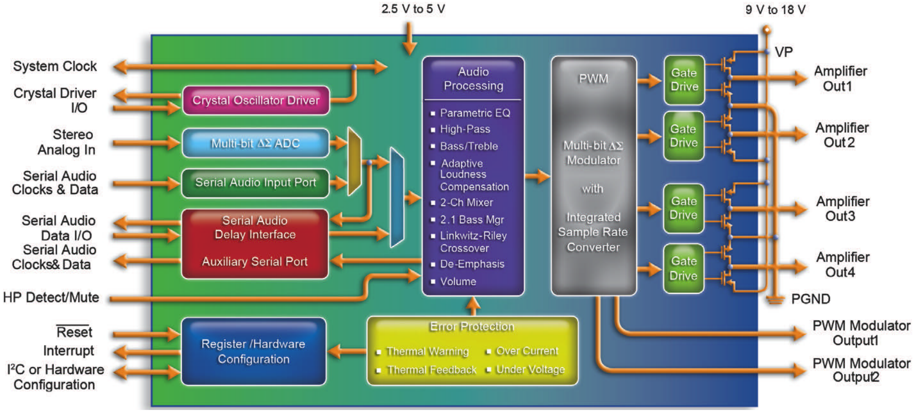


CS4525

CS4525 and CS4412 Applications

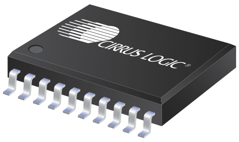
- Integrated digital TVs
- Flat-panel TV monitors
- Computer/TV monitors
- Mini/micro shelf systems
- Powered speakers
- Portable docking stations
- Computer desktop audio

Digital Amplifiers Power Stages

Part	Power	Dynamic Range	THD+N	Channels	Power Supply	Comments	Package
CS4525	30 W	102 dB	0.1%	2.1	VP = 9 V to 18 V; VD = 2.5 V to 5 V	Integrated Digital Audio Amplifier with ADC, SRC, and Signal Processor	48 QFN
CS4412	30 W	102 dB	0.1%	4	VP = 9 V to 18 V; VD = 2.5 V to 5 V	Quad Power Stage IC Thermally Enhanced 85% Efficiency	48 QFN
CS44130	60 W	107 dB	0.12%	4	VP = 10.8 V to 21 V; VD = 3.3 V or 5 V; VL = 2.5 V to 5 V	Quad Power Stage IC Thermally Enhanced 90% Efficiency	48 QFN
CS44600	N/A	100 dB	<0.05%	6	VD = 2.5 V; VL = 3.3 V to 5 V	192 kHz Digital Amplifier Controller	64 LQFP
CS44800	N/A	100 dB	<0.05%	8	VD = 2.5 V; VL = 3.3 V to 5 V	192 kHz Digital Amplifier Controller	64 LQFP

CS4525 Features

- Fully integrated power amplifier
  - Stereo A/D converter
  - Asynchronous serial data interface
  - Sample-rate converter
  - Digital audio processor
  - PWM controller
  - Power MOSFETs
- No heatsink required
  - Programmable power foldback on thermal warning
  - High efficiency
- Built-in protection with error reporting
  - Overcurrent/undervoltage/thermal overload shutdown
  - Thermal warning reporting
- >100 dB dynamic range
- <0.1% THD+N @ 1 W
- Configurable outputs (10% THD+N)
  - 1 x 30 W into 4 Ω, parallel full-bridge
  - 2 x 15 W into 8 Ω, full-bridge
  - 2 x 7 W into 4 Ω, half-bridge +1 x 15 W into 8 Ω, full-bridge
- PWM Popguard® technology for half-bridge mode
- Programmable channel delay and spread spectrum PWM modulation for system noise and radiated emissions management
- On-chip stereo A/D converter
  - 24-bit, 48 kHz conversion
  - 95 dB dynamic range, –88 dB THD+N
  - 2 V_{RMS} input supports SCART
- Thermally enhanced QFN package; lead-free assembly



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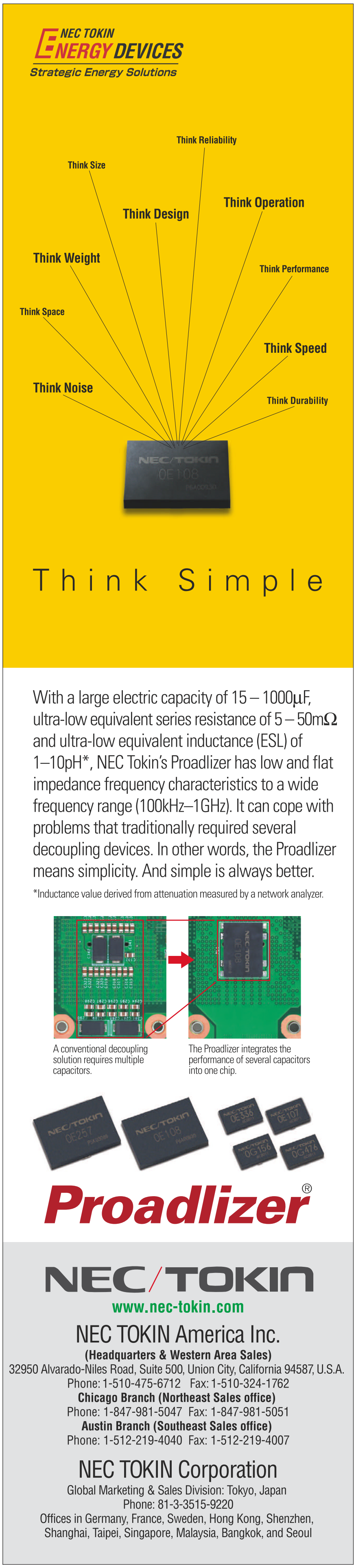

CONSIDER THE SIZE, FOCUS, BANDWIDTH OFFERINGS, AND MOTIVATION OF THE IP VENDOR.

categories (**Table 1**). The HIP is also customizable so that even semiconductor companies or foundries can add their own versions of the tool to their IP repositories. The HIP scores also allow users to compare as many as 20 cores on one scorecard and allow vendors and suppliers to securely share data. To date, however, the tool supports only hard IP.

So, although neither an ISO 9000-type standard nor a master IP repository exists for all types of IP, designers can converge on a choice using several resources. Like the four Cs of judging a diamond—color, cut, clarity, and carat, the four Cs of cores—compare, consider, collect, and calculate—will help designers narrow their choices and more easily locate the core that will help them quickly complete their designs.

COMPARE MANY CORES

The first stop for any design group should be its own internal library. If you have used an in-house core, it's a no-brainer to use it again. If your company has a core but doesn't have the documentation, including the models, testbenches, and drivers, and is no longer employing the architect of the core, experts strongly suggest you consider looking outside the company. If you go with undocumented IP, you won't have a licensing fee, but you'll likely end up redesigning the core. Years ago, a Motorola executive bemoaned the fact that his company had three PCI cores in-house and still went outside to license a PCI core from Phoenix Technologies, whose IP group Synopsys now owns. Motorola had abandoned the other cores because it hadn't yet established an IP repository and a way to catalog its own IP, so the company ultimately chose to license its cores.

If you lack an in-house core, you can look for a core in your targeted ASIC company, foundry, or FPGA company. They all have a vested interest in seeing you design successfully and hit market windows, so that you can ramp to massive volume production and ultimately pay them. Therefore, the FPGA companies, ASIC companies, and, more recently, foundries, such as TSMC (Taiwan Semiconductor Manufacturing Co), UMC (United Microelectronics Corp), and the Chartered/Samsung/Infineon common-platform alliance, have built vast repositories of IP. Many of the silicon manufacturers even recommend vendors and sometimes assist you in finding the right IP.

You can also tap one of your EDA vendors. The big-three EDA vendors—Cadence, Synopsys, and Mentor—all have large IP libraries. Analysts often rank Synopsys as one of the top-three IP suppliers, because it has over the last 10 years accumulated a massive soft-core portfolio through development and acquisition. For those designers who own tools, some EDA vendors may provide free or nominally priced IP. As cores age, they often become commodity macro functions in synthesis libraries. Before you decide to choose an EDA or a semiconductor company's IP, look around and weigh all your options. A good way to get a feel for most of the cores available is by checking out the online IP catalogs at sites such as Design & Reuse and Chip Estimate. Both sites list multiple IP vendors and their offerings and allow users to compare IP by type. Users can get an idea of which vendors offer what IP. Because there is growing competition in the IP-catalog area, these sites will likely start to pro-

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⊞ For more on IP (intellectual property) in the worldwide market, check out our Global Report at www.edn.com/article/CA6387029.

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⊞ Sister publication *Electronic News* examines the IP market at www.edn.com/article/CA475606.

⊞ Go to www.edn.com/070201cs and click on Feedback Loop to post a comment on this article.

vide more in-depth information to help you narrow your choices.

CONSIDER VENDOR SIZE

After you have a lay of the land and know which vendors offer which cores, consider the size, focus, bandwidth offerings, and motivation of the IP vendor. Typically, large, successful IP vendors consistently offer quality products. Star-IP vendors, such as ARM, MIPS, Virage Logic, Tensilica, and ARC, live on the success of their customers. Like the foundries and ASIC companies, they have a vested interest in ensuring that their customers succeed. Most of these star-IP vendors demand a per-chip royalty, and they don't receive that royalty if you don't sell your products. Thus, they tend to provide customers with testbenches, regression suites, and even embedded software to help them quickly finish designs and proceed to volume production and royalty payments.

Things get a bit dicey when you're dealing with less well-known, smaller companies. All IP vendors would like to garner a royalty, but most customers would rather not pay one and much prefer one-time perpetual licensing or even single-project licenses. But if an IP vendor isn't gathering a royalty, it doesn't have a stake in the end game and tends to be less enthusiastic about supporting customers after they have signed the licensing agreement.

At this point, you need to consider the size of the company and, more important, the bandwidth it offers. Many small IP vendors are design-services companies that have developed a block of IP in the course of their design services. It's important for you to consider whether the vendor's primary business is IP or design services. A general rule of thumb is that if the vendor's main business is design services, the IP core on its own will tend to be of lower quality, but the support and extra services will tend to be better than those of vendors whose main business is IP licensing. And, conversely, if the vendor's primary business is licensing IP, it tends to deliver a well-rounded IP-deliverables package, including testbenches, models, and regression suites, but typically lacks in application knowledge and support. If you are licensing a digital core, check that the vendor has thoroughly verified the core and that it has undergone several regression tests in the application you are targeting.

"An IP vendor can do only a limited job of verifying IP," said an attendee at the FSA's Fall 2006 IP conference. "One thing they cannot do well is verify in the context of the application of that end user. A good IP vendor will develop a regression suite that grows over time, adding more applications to it as they work with more customers. A customer would do well to figure out what exactly is in their regression suite. If the suite encompasses the customer's application, then the customer has to do less reverification. If not, work with the IP vendor, and the vendor will add that regression suite to its IP for future designs."

Tobias notes that, if you are licensing analog IP, it is even more important that the IP vendor has the bandwidth to help the customer with the design. "Analog tends to be sensitive, but, when the cores aren't even designed properly in the first place, it can become a nightmare," says Tobias.

COLLECT REFERENCES

Most designers learn about the quality of cores through word of mouth. If you are new to an application and are trying a core that you don't know, ask around. Ask the IP vendor for a reference. If the vendor refuses to give you one, you can usually find a press release or even find customer logos on the company's Web site. The IC-design business is relatively small, and chances are you'll know someone in the company or someone at your company knows a designer at the company. If you are successful and contact the designer, you can ask the designer general questions about the quality of the core and vendor support. You can also check out various user groups or chat groups on Design & Reuse's and Chip Estimate's Web sites.

It's important to ask how the core functions, whether the designers had to perform reverification—or, more likely, how much—what came with the deliverables, and whether the IP vendor was helpful once the customer received the core. It is also helpful to ask wheth-

MOST DESIGNERS LEARN ABOUT THE QUALITY OF CORES THROUGH WORD OF MOUTH.

er the core complies with the SPIRIT (structure for packaging, integrating, and reusing IP within tool flows) standard. The SPIRIT Consortium comprises companies dedicated to the adoption of a unified set of specifications for configuring, integrating, and verifying IP in advanced SOC-design tool sets. If the cores you are evaluating are SPIRIT-compliant, you're in good shape so far.

CALCULATE RISKS

If, after taking these steps, you end up with a short list of potential vendors, ask them for their VSIA QIP grade or FSA HIP data. Although VSIA may not have the momentum or the huge membership it once did, the organization is still going strong and is still improving the QIP. Even if a vendor is not an official or active member of VSIA, any one that is worth its salt has a QIP grade for its IP. The IP industry doesn't have an official industry organization, like EDA has with EDAC (Electronic Design Automation Consortium) or fabless companies have with the FSA. VSIA is the closest thing, so IP vendors have most likely filled out the QIP form simply to see how they stack up.

You should base your decision neither solely on the QIP nor strictly on the criteria. Critics point out that QIP tends to be strong in verifying that a design is functionally correct and has a solid deliverables package. It tends to be weaker in looking at application-specific issues and communications-standards conformance. It also assigns one score to certain criteria about which you may be unconcerned. Still, it doesn't hurt to check it out or even suggest improvements to the VSIA's QIP group.

For hard IP, you should also check out FSA's new HIP-assessment tool, which is available free for downloading at www.fsa.org/committees/ip/hardip.asp. The tool currently focuses on hard IP, but the FSA may extend it to also cover soft and verification IP. FSA is also seeking a partnership with Chip Estimate to offer IP evaluation through Chip Estimate's site, but has not yet released details.

The IP industry has enabled the SOC revolution, yet it still hasn't reached its full potential. It could get there by participating more fully in defining industry standards and maybe even forming into its own industry. As PMC-Sierra's Driesing noted at the FSA panel, if IP vendors spent more time increasing the quality of their IP before releasing the cores, they could probably garner higher licensing fees. Then, by 2016, the IP industry may be able to afford fireworks and a comedian. I'd like to be there. In the meantime, when mining for IP, remember the four Cs: compare, consider, collect, and calculate.**EDN**

FOR MORE INFORMATION

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Chartered Semiconductor	www.charteredsemi.com
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BY JIM WILLIAMS • LINEAR TECHNOLOGY CORP

Designing instrumentation circuitry with rms/dc converters

RMS CONVERTERS RECTIFY AVERAGE RESULTS.

Using rms to measure waveforms furnishes the most accurate amplitude information (**Reference 1**). Rectify-and-average schemes, which you usually calibrate to a sine wave, are accurate for only one waveshape, however. Departures from this waveshape result in pronounced errors. Although accurate, rms conversion often entails limited bandwidth, restricted range, complexity, and difficult-to-characterize dynamic and static errors. Recent developments address these issues and also improve accuracy. **Table 1** at the Web version of this article at www.edn.com/ms4228 shows Linear Technology's (www.linear.com) LTC1966/LTC1967/LTC1968 device family. The devices feature low-frequency accuracy, including linearity and gain error, of 0.5% and 1% error at bandwidths extending to 500 kHz. These converters employ a sigma-delta-based computational scheme to achieve their performance.

Figure 1's pinout descriptions and basic circuits reveal an easily applied device. An output filter capacitor is all that is necessary to form a functional rms/dc converter. The **figure** shows split- and single-supply-powered variants. Such ease of implementation invites a broad range of application; examples begin with **Figure 2**.

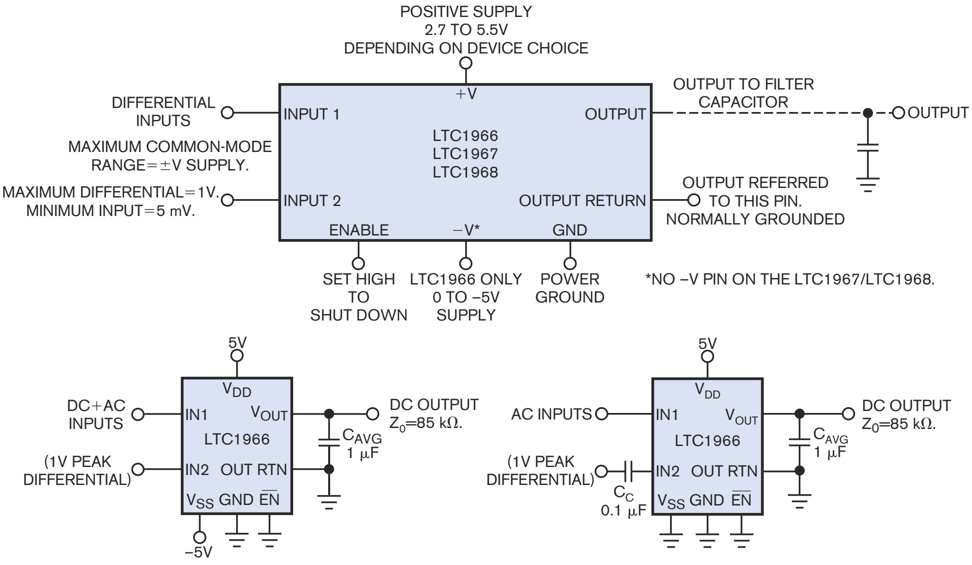

Figure 1 The pinout descriptions (top) and basic circuits (bottom) include the rms converter's pin functions and application circuits. The pins' descriptions are equivalent in all the devices, with only minor differences.

ISOLATED POWER-LINE MONITOR

Figure 2's ac-power-line monitor has 0.5% accuracy over a sensed 90 to 130V-ac input and provides a safe, fully isolated output. Conversion of rms provides accurate reporting of ac-line voltage, regardless of waveform distortion, which is common. T_1's ratio divides down the ac-line voltage. An isolated and reduced potential appears across T_1's secondary, B, at which it resistively scales and presents itself to IC_1's input. Power for IC_1 comes from T_1's secondary, A, which you rectify, filter, and zener-regulate to dc. IC_2 provides a numerically convenient output from gain. You can increase accuracy by biasing T_1 to an optimal loading point, which the relatively low-resistance-divider values facilitate. Similarly, although IC_1 and IC_2 can operate from one supply, split supplies maintain symmetrical T_1 loading. You calibrate the circuit by adjusting the 1-kΩ trim for 1.20V output with the ac line at 120V ac. You make this adjustment using a variable-ac-line transformer and a floating rms voltmeter (see **sidebar** "AC-measurement and signal-handling practice" at the Web version of this article at www.edn.com/ms4228 for recommendations on rms voltmeters and other ac-measurement-related gossip).

Figure 3's error plot shows 0.5% accuracy from 90 to 130V ac, degrading to 1.4% at 140V ac. The beneficial effect of trimming at 120V ac is evident; trimming at full-scale would result in larger overall error, primarily due to nonideal-transformer behavior. Note that the data is specific to the transformer. Substitution for T_1 necessitates circuit-value changes and recharacterization.

FULLY ISOLATED

RMS/dc converters commonly require accurate rms-amplitude measurement of an SCR's (silicon-controlled rectifier's) chopped ac-line waveforms. The

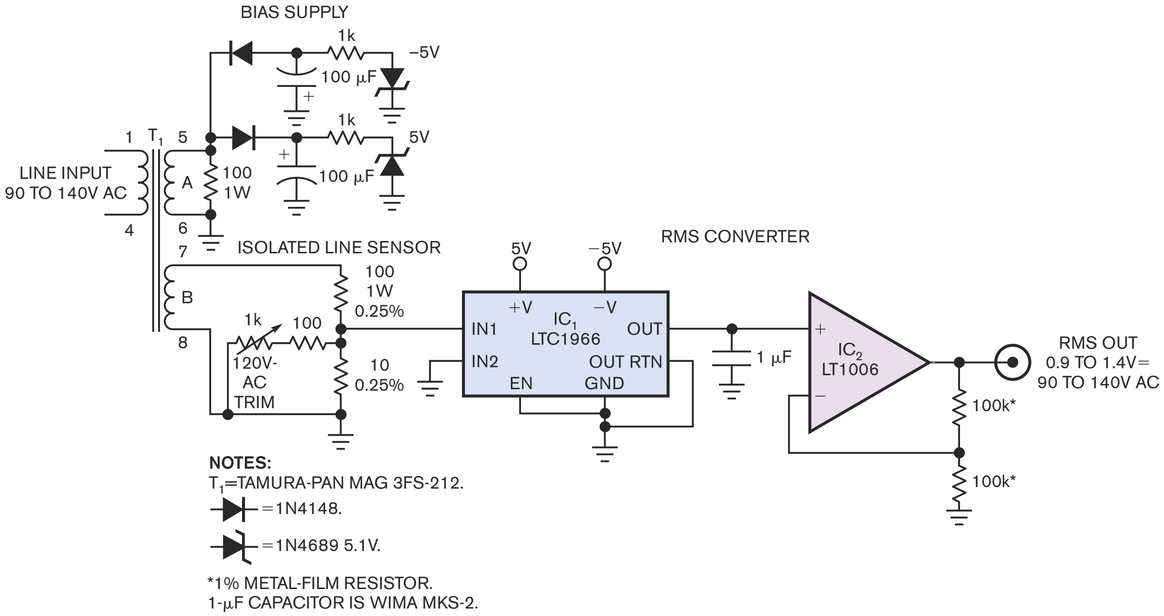

Figure 2 This isolated power-line monitor senses with a transformer and provides 0.5% accuracy from 90 to 130V-ac input. Loading the transformer secondary optimizes the voltage conversion's linearity.

SCR's fast sine-wave switching complicates this measurement because this speed introduces odd waveshapes with high-frequency harmonic content. **Figure 4**'s conceptual SCR-based ac/dc converter is typical. The SCRs alternatively chop the 220V-ac line, responding to a loop-enforced, phase-modulated trigger to maintain a dc output. **Figure 5**'s waveforms show typical operation. Trace A represents one ac-line phase, and Trace B represents the SCR cathodes. The SCR's irregularly shaped waveform contains dc and high-frequency harmonics, requiring wideband rms conversion for measurement. Additionally, for safety and system-interface considerations, you must fully isolate the measurement.

Figure 6 provides isolated power and data-output paths to an rms/dc converter, permitting safe, wideband, digital output-rms

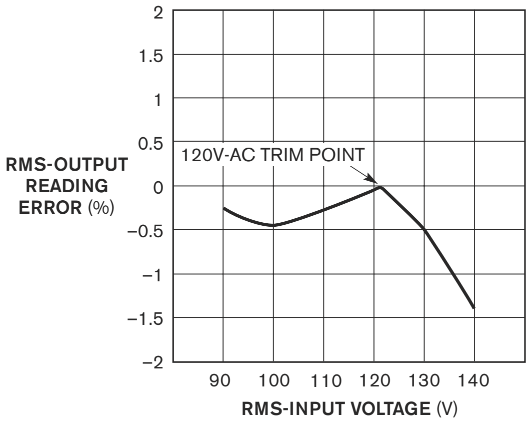

Figure 3 The line monitor has 0.5% accuracy from 90 to 130V ac, degrading to 1.4% accuracy at 140V ac. Almost all the error is due to transformer parasitic losses.

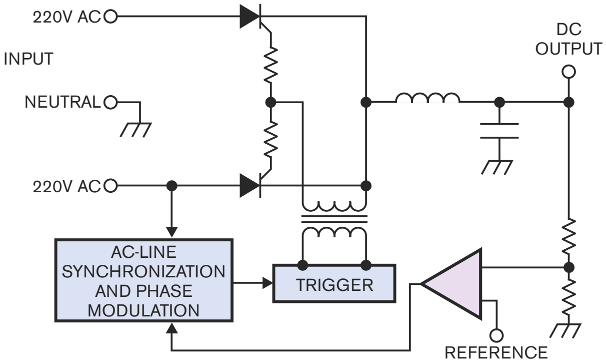

Figure 4 This ac/dc converter is typical of SCR-based designs. Feedback directs the SCR, which synchronizes with the ac line. The SCR's trigger-phase modulation controls the dc output.

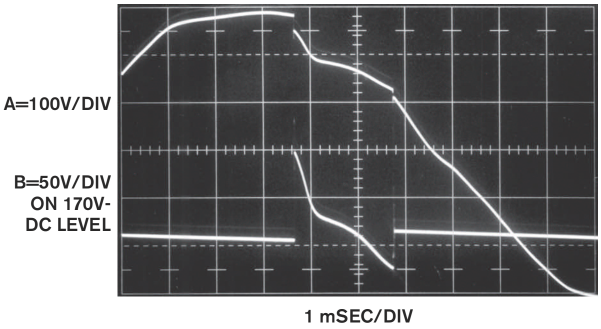

Figure 5 Trace A is the ac line of the SCR-based ac/dc converter. Trace B is the waveform at the SCR cathode. It contains dc and high-frequency harmonics that require wideband rms measurement to ensure accurate regulation.


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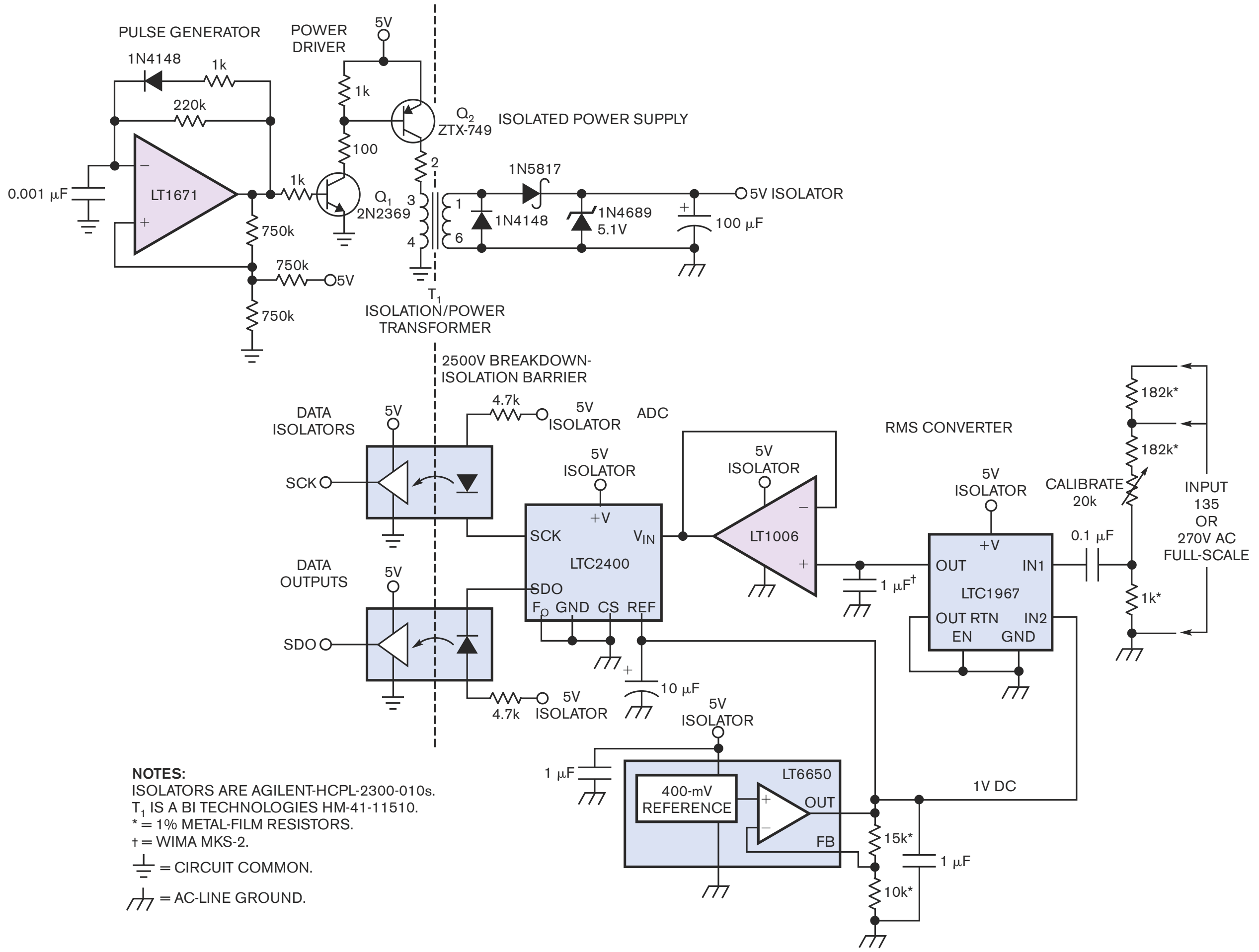
Firmware Changes



NOTES:
ISOLATORS ARE AGILENT-HCPL-2300-010s.
T_1 IS A BI TECHNOLOGIES HM-41-11510.
* = 1% METAL-FILM RESISTORS.
† = WIMA MKS-2.
= CIRCUIT COMMON.
= AC-LINE GROUND.

Figure 6 Optoisolators provide a safe, low-voltage digital output for this wideband-rms-measurement circuit. T_1 and associated circuitry provide isolated power for the rms converter, and a resistive divider performs high-voltage ac sensing. An ADC provides a serial output to the optoisolators. The accuracy of this circuit is 1% over a 200-kHz bandwidth.

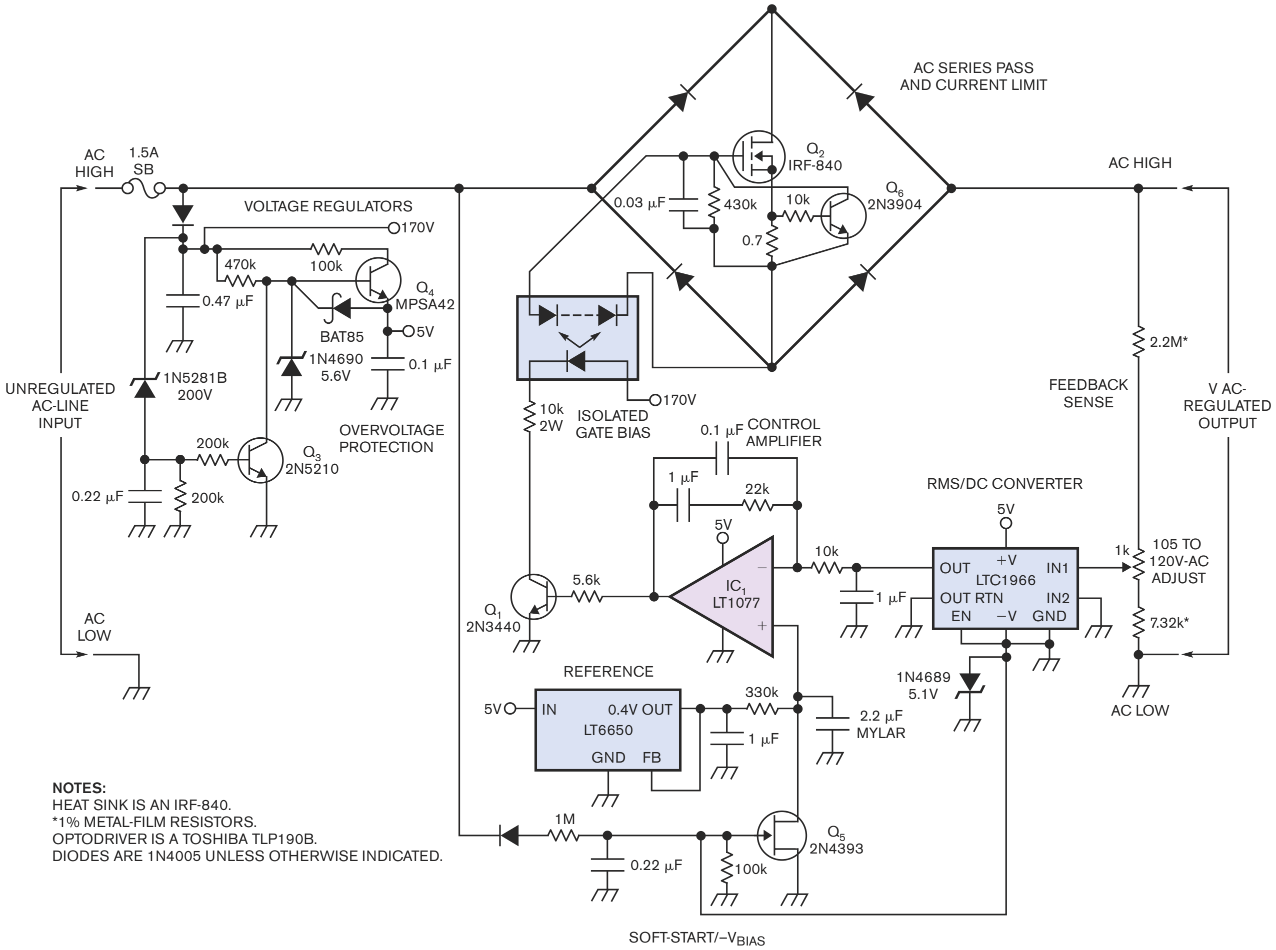
measurement. A pulse-generator-configured comparator combines with Q_1 and Q_2 to drive T_1, resulting in isolated 5V power at T_1's rectified, filtered, and zener-regulated output. The rms/dc converter senses either 135 or 270V-ac full-scale inputs through a resistive divider. The converter's dc output feeds a self-clocked, serially interfaced ADC; optocouplers convey output data across the isolation barrier. The LTC6650 provides a 1V reference to the ADC and biases the rms/dc converter's inputs to accommodate the voltage divider's ac swing. You accomplish calibration by adjusting the 20-kΩ trim and noting that output data agrees with the input ac voltage. Circuit accuracy is within 1% in a 200-kHz bandwidth.

LOW-DISTORTION AC-LINE RMS REGULATOR

Almost all functioning ac-line-voltage regulators rely on some form of waveform chopping, clipping, or interruption. This requirement promotes efficiency but introduces waveform distortion, which is unacceptable in some applications. **Figure 7** regulates the ac line's rms value within 0.25% over wide input swings and introduces no distortion. It accomplishes this task by continuously controlling the conductivity of a series-pass MOSFET in the ac line's path. Enclosing the MOSFET in a diode bridge permits it to operate during both ac-line polarities.

You apply the ac-line voltage to the Q_2-diode bridge. A calibrated variable-voltage divider senses this bridge and feeds IC_1. You route IC_1's output, representing the regulated line's rms value, to control amplifier IC_2 and compare it with a reference. IC_2's output biases Q_1, controlling drive to a photovoltaic optoisolator. The optoisolator's output voltage provides level-shifted bias to diode-bridge-enclosed Q_2, closing a control loop, which regulates the output's rms voltage against ac-line and -load shifts. RC components in IC_2's local feedback path stabilize the control loop. The loop operates Q_2 in its linear region, much like a common low-voltage dc linear regulator. The result is the absence of introduced distortion at the expense of lost power. Heat dissipation constrains the available output power. For example, when you set the output adjustment to regulate 10V below the normal input, Q_2 dissipates about 10W at 100W output. You can improve this figure, however. The circuit regulates for $V_{IN} \geq 2V$ above V_{OUT}, but operation in this region risks regulation dropout as V_{IN} varies.

Circuit details include JFET Q_5 and associated components. The passive components associated with Q_5's gate form a slow



NOTES:
HEAT SINK IS AN IRF-840.
*1% METAL-FILM RESISTORS.
OPTODRIVER IS A TOSHIBA TLP190B.
DIODES ARE 1N4005 UNLESS OTHERWISE INDICATED.

Figure 7 This ac-line-voltage regulator introduces no waveform distortion. IC_2 senses the rms value of line voltage and compares it with a reference. IC_2 then biases the photovoltaic optocoupler through Q_1. Q_2 sets the diode bridge's conductivity and closes the control loop. The input voltage must be 2V higher than the output voltage to maintain regulation.

turn-on negative supply for IC_1. They also provide gate bias for Q_5, a soft-start transistor that prevents abrupt ac power application to the output at start-up. When power is off, Q_5 conducts, holding IC_2's positive input low. When you apply power, IC_1 initially has a 0V reference, causing the control loop to set the output at zero. As the 1 MΩ, 0.22-µF combination charges, Q_5's gate moves negative, causing its channel conductivity to gradually decay. Q_5 ramps off, IC_2's positive input moves smoothly toward the LT6650's 400-mV reference, and the ac output similarly ascends toward its regulation point. Current sensor Q_6, measuring across the 0.7Ω shunt, limits output current to approximately 1A. At normal line inputs of 90 to 135V ac, Q_4 supplies 5V operating bias to the circuit. If line voltage rises beyond this point, Q_3 comes on, turning off Q_4 and shutting down the circuit.

GAIN-OF-1000 PREAMPLIFIERS

The preceding circuits furnish high-level inputs to the rms converter. Many applications lack this advantage and require some form of preamplifier. High gain preamplification for the rms converter requires more attention than you might suppose. The preamplifier must have low offset error because the rms converter (desirably) processes dc as legitimate input. More subtly, the preamplifier must have far more bandwidth than is immediately apparent. The amplifier's −3-dB bandwidth is of interest, but its closed-loop 1%-amplitude-error bandwidth must be high enough to maintain accuracy over the rms converter's 1%-error passband. This requirement is not trivial, because very high open-loop gain at the maximum frequency of interest is necessary to avoid inaccurate closed-loop gain.

Figure 8 shows a gain-of-1000 preamplifier that preserves the LTC1966's dc to 6-kHz, 1% accuracy. The amplifier may be either ac- or dc-coupled to the rms converter. The 1-mV full-scale input splits into high- and low-frequency paths. IC_1 and IC_2, which are both ac-coupled, take a cascaded, high-frequency gain of 1000. Chopper-stabilized IC_3 which is dc-coupled, also has a gain of 1000, but its RC-input filter restricts it to operate only at dc and low frequency. Assuming the switch is set to dc+ac, high- and low-frequency-path information recombine at the rms converter. The high-frequency path's 650-kHz, −3-dB response combines with the low-frequency section's microvolt-level offset to preserve the rms converter's dc to 6-kHz 1% error. If you require only ac response, set the switch to the appropriate position. The minimum processable input, which the circuit's noise floor sets, is 15 µV.

The LTC1968, with a 500-kHz, 1%-error bandwidth, poses a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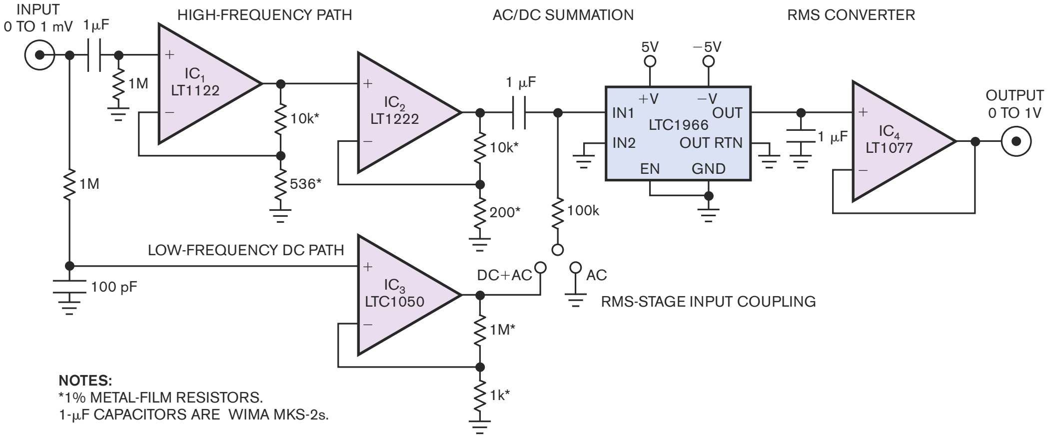
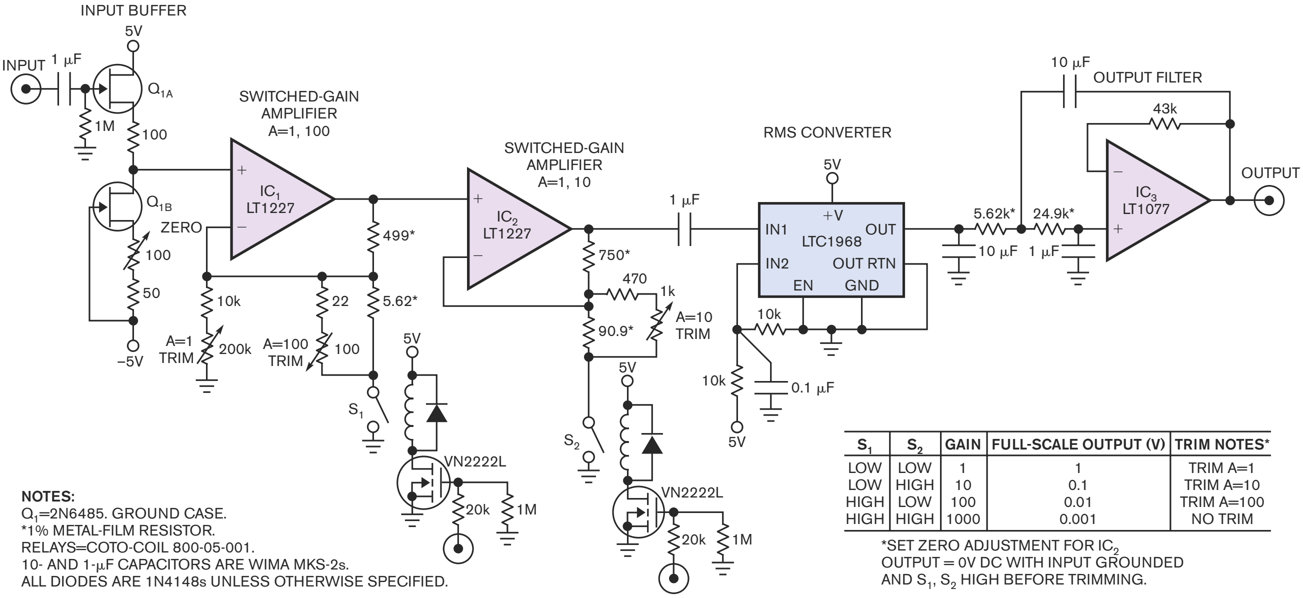


NOTES:
*1% METAL-FILM RESISTORS.
1-µF CAPACITORS ARE WIMA MKS-2s.

Figure 8 This gain-of-1000 preamplifier allows rms-to-dc conversion with 1-mV full-scale sensitivity. The input splits into high- and low-frequency paths that recombine at the rms converter. The amplifier's 650-kHz, −3-dB bandwidth preserves the rms converter's 6-kHz, 1%-error bandwidth. The noise floor of this circuit is 15 µV.



S$_1$	S$_2$	GAIN	FULL-SCALE OUTPUT (V)	TRIM NOTES*
LOW	LOW	1	1	TRIM A=1
LOW	HIGH	10	0.1	TRIM A=10
HIGH	LOW	100	0.01	TRIM A=100
HIGH	HIGH	1000	0.001	NO TRIM

*SET ZERO ADJUSTMENT FOR IC$_2$
OUTPUT = 0V DC WITH INPUT GROUNDED
AND S$_1$, S$_2$ HIGH BEFORE TRIMMING.

NOTES:
Q$_1$=2N6485. GROUND CASE.
*1% METAL-FILM RESISTOR.
RELAYS=COTO-COIL 800-05-001.
10- AND 1-µF CAPACITORS ARE WIMA MKS-2s.
ALL DIODES ARE 1N4148s UNLESS OTHERWISE SPECIFIED.

Figure 9 This switched-gain, 10-MHz, −3-dB ac preamplifier preserves the LTC1968's 500-kHz, 1%-error bandwidth. The decade-ranged gains allow a 1-mV full-scale reading with a 20-µV noise floor. The JFET-input stage provides high input impedance. AC coupling and a third-order Sallen-Key filter maintain 1% accuracy down to 10 Hz.

significant challenge for an accurate preamplifier, but the circuit in **Figure 9** meets the requirement. This design features decade-ranged gain to 1000 with a 1%-error bandwidth beyond 500 kHz, preserving the rms converter's 1%-error bandwidth. Its 20-µV noise floor maintains wideband performance at microvolt-level inputs. Q$_{1A}$ and Q$_{1B}$ form a low-noise buffer, permitting high-impedance inputs. IC$_1$ and IC$_2$, which are both gain-switchable, take cascaded gain in accordance with the **figure**'s table. You set the gains using reed relays, which a 2-bit code controls. IC$_2$'s output feeds the rms converter, and a Sallen-Key active filter smoothes the converter's output. The circuit maintains 1% error over a 10-Hz to 500-kHz bandwidth at all gains due to the preamplifier's −3-dB, 10-MHz bandwidth. You can eliminate the 10-Hz, low-frequency restriction with a dc-stabilization path similar to the one in **Figure 8**, but you would have to switch its gain in concert with the IC$_1$-IC$_2$ path.

Figure 10 shows preamplifier response to a 1-mV input step at a gain of 1000. IC$_2$'s output is singularly clean, with trace thickening in the pulse's flat portions due to the 20-µV noise floor. The 35-nsec rise time indicates a 10-MHz bandwidth. To calibrate this circuit, first set S$_1$ and S$_2$ high, ground the input, and trim the zero adjustment for 0V dc at IC$_2$'s output. Next, set S$_1$ and S$_2$ low, apply a 1V, 100-kHz input, and trim A=1 for unity gain, which you measure at the circuit output, in accordance with the table in **Figure 9**. Continue this procedure for the remaining three gains in the table. A good way of generating the required accurate low-level inputs is to set a 1V-ac lev-

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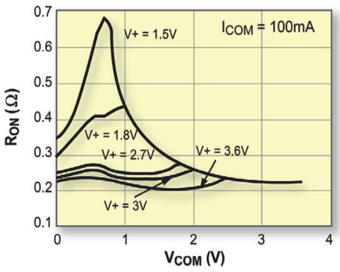
Singles	ISL84714	SPDT/2:1 Mux	0.44	0.06	6kV	1.6 to 3.6	SC70-6
	ISL84715	SPST (NO)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL84716	SPST (NC)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL43L210	SPDT/2:1 Mux	0.44	0.06	6kV	1.1 to 4.5	SC70-6
	ISL43L110	SPST (NO)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
	ISL43L111	SPST (NC)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
Duals	ISL84762	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL84684	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL8484	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 4.5	TDFN, MSOP
	ISL43L220	2xSPDT/2:1 Mux	0.23	0.03	9kV	1.1 to 4.5	TDFN
	ISL43L410	DPDT/Diff 2:1 Mux	0.29	0.03	9kV	1.1 to 4.5	TDFN, MSOP
	ISL43L120	SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L121	SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L122	SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L710	Diff SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L711	Diff SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L712	Diff SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
Quads	ISL83699	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 3.6	QFN, TSSOP
	ISL84780	Dual DPDT/Diff 2:1 Mux	0.45	0.07	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL8499	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 4.5	QFN, TSSOP
	ISL43L420	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.1 to 4.5	QFN
Octals	ISL84781	8:1 Mux	0.41	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL84782	Diff 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL43L840	Dual 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	QFN, TSSOP
	ISL43L841	Diff: 4:1 Mux	0.5	0.056	4kV	1.6 to 4.5	TQFN, TSSOP

ISL84684 Typical Performance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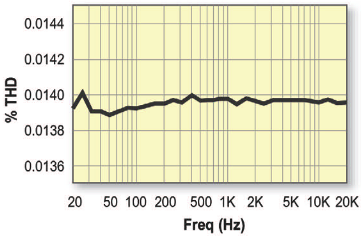
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el and divide it down with a high-grade 50Ω attenuator, such as the Hewlett-Packard (www.hp.com) 350D or the Tektronix (www.tektronix.com) 2701. It is prudent to verify the attenuator's output with a precision rms voltmeter (see **sidebar** "AC-measurement and signal-handling practice" at the Web version of this article at www.edn.com/ms4228).

MEASURING QUARTZ-CRYSTAL RMS CURRENT

Quartz-crystal rms operating current is critical to long-term stability, temperature coefficient, and reliability. You must minimize introduced parasitics, particularly capacitance, which corrupt crystal operation. This requirement complicates accurate determination of rms-crystal current. **Figure 11**, a form of **Figure 9**'s wideband amplifier, combines with a commercially available closed-core current probe to permit the measurement. An rms/dc converter supplies the rms value. The quartz-crystal test circuit in dashed lines exemplifies a typical measurement situation. The Tektronix CT-2 current probe monitors crystal current and introduces minimal parasitic loading. The probe's 50Ω termination allows direct connection to IC_1 without the FET buffer in **Figure 9**. Additionally, because quartz crystals are uncommon at frequencies lower than 4 kHz, IC_1's gain does not extend to low frequency.

Figure 12 shows the results. A crystal drive, which you take at Q_1's collector (Trace A), causes a 25-μA-rms crystal current, which appears at the rms/dc-converter input (Trace B). The trace enlargement is due to the preamplifier's 5-μA-rms equivalent-noise contribution. **Table 2** at the Web version of this article at www.edn.com/ms4228 details characteristics of two Tektronix closed-core current probes. The primary trade-off is low-frequency error versus sensitivity. The current probes contribute essentially no probe noise, and capacitive loading is notably low. You calibrate the circuit by putting 1-mA rms current through the probe and adjusting the indicated trim for a 1V circuit output. To generate the 1 mA, drive a 1-kΩ, 0.1% resistor with 1V rms.

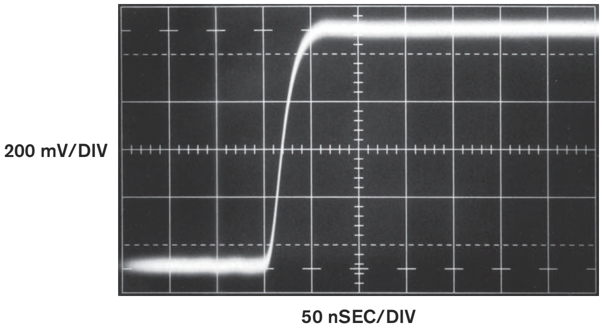

Figure 10 IC_2 in Figure 9 responds to a 1-mV input step with a gain of 1000. The 35-nsec rise time indicates the 10-MHz bandwidth. The thickened trace at the flat portions of the pulse represents the noise floor.

STABLE AC-VOLTAGE STANDARD

Figure 13 uses the rms/dc converter's stability in an ac-voltage standard. Initial circuit accuracy is 0.1%, and six months of drift at 20 to 30°C remains within that figure. Additionally, the 4-kHz operating frequency is within 0.01%, and distortion is less than 30 ppm. IC_1 and its power buffer, IC_3, sense across a bridge comprising a 4-kHz quartz crystal and an RC impedance in one arm; resistors and an LED-driven photocell comprise the other arm. IC_1 sees positive feedback at the crystal's 4-kHz resonance, promoting oscillation. Negative feedback, stabilizing oscillation amplitude, occurs through a control path, which includes an rms/dc converter and an amplitude-control amplifier, IC_5. IC_5 acts on the difference between IC_3's rms-converted output and the LT1009 voltage reference. Its output controls the LED-driven photocell to set IC_1's negative feedback. RC components in IC_5's feedback path stabilize the control loop. The 50-kΩ trim sets the optically driven resistor's value to the point at which IC_3's lowest output distortion occurs and maintains adequate loop stability.

Normally, you would ground the bridge's "bottom." Although this connection works, it subjects IC_1 to common-mode swings, increasing distortion due to IC_1's finite common-mode rejection versus frequency. IC_2 eliminates this concern

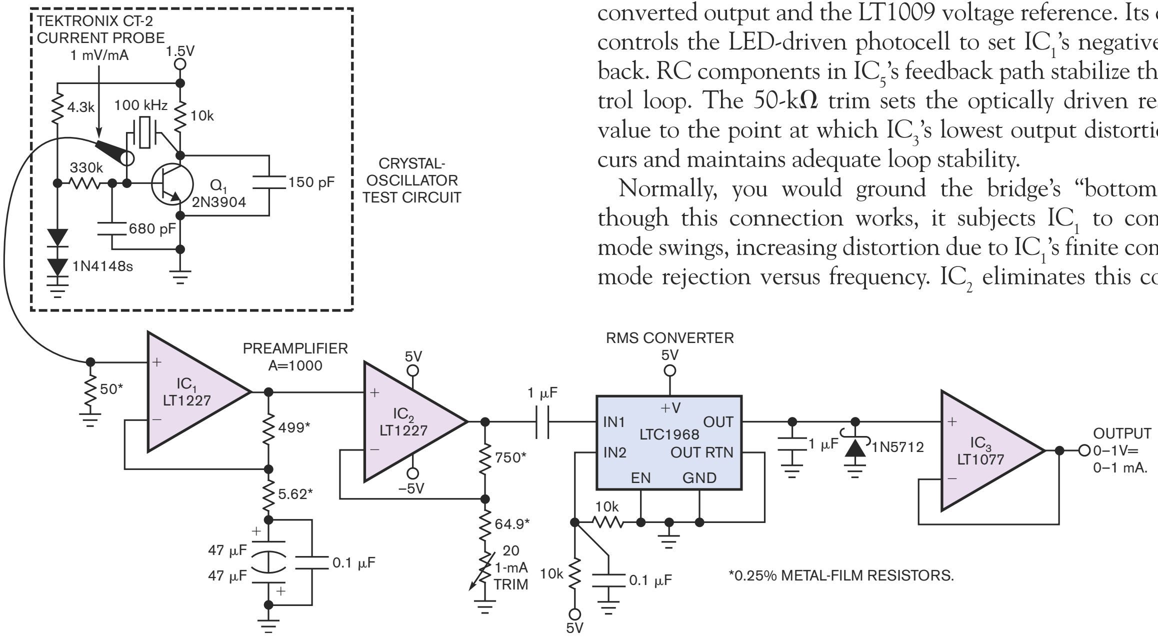

Figure 11 The circuit of Figure 9 adapts to the isolated true-rms measurement of the current in a quartz crystal. The current probe's 50Ω impedance allows the elimination of the FET-input buffer and direct connection to IC_1. The current probe does not appreciably load the crystal in this oscillator test circuit.

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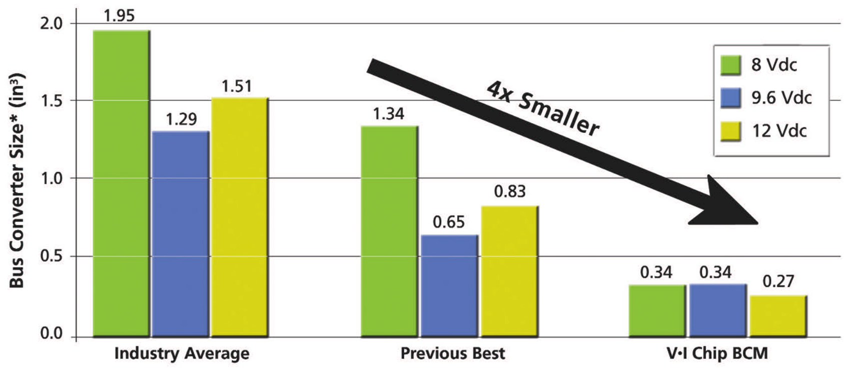

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The 4-kHz crystal is a relatively large structure with a high Q factor. Normally, it would require more than 30 sec to start and arrive at full, regulated amplitude. You avoid this drawback by including the Q1-LTC201-switch circuitry. At start-up, IC_5's output goes high, biasing Q_1. Q_1's collector goes low, turning on the LTC201. This action sets IC_1's gain abnormally high, increasing bridge drive and accelerating crystal start-up. When the bridge arrives at its operating point, IC_5's output drops to a lower value, Q_1 and the LTC201 switch off, and the circuit moves into normal operation. Start-up time is several seconds.

The circuit requires trimming for amplitude accuracy and lowest distortion. You perform the distortion trim first. Adjust the trim for minimal output distortion, which you measure on a distortion analyzer. Note that the absolute lowest level of distortion coincides with the point at which control-loop gain is just adequate to maintain oscillation. As such, find this point and retreat from it into the control loop's active region. This retreat necessitates giving up about 5-ppm distortion, but you can achieve 30 ppm with good control-loop stability. You trim output amplitude with the indicated adjustment for exactly 1.414V rms (2V peak) at the circuit output.

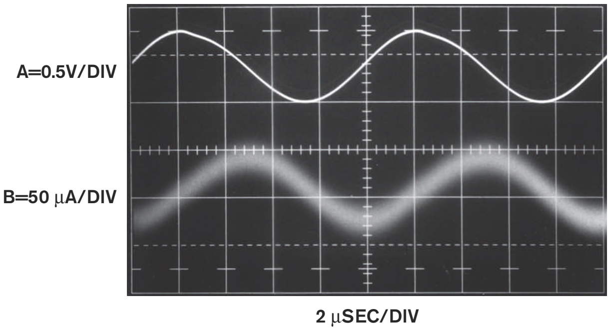

Figure 12 Trace A shows the crystal voltage, and Trace B shows the crystal current for the circuit in Figure 11. The 25-µA rms-crystal-current measurement includes the 5-µA noise-floor contribution of the preamplifier.

RANDOM-NOISE GENERATOR

Figure 15 uses the rms/dc converter in a leveled-output-random-noise generator. Noise diode D_1 ac-biases IC_1, operating at a gain of two. IC_1's output feeds a 1- to 500-kHz, switch-selectable lowpass filter. The filter output-biases the variable-gain amplifier, IC_2-IC_3. IC_2, a current-controlled transconductance amplifier, and IC_3, an output amplifier, reside on one chip. This stage takes ac gain, biases the LTC1968 rms/dc converter, and acts as the circuit's output. The rms-converter output at IC_4

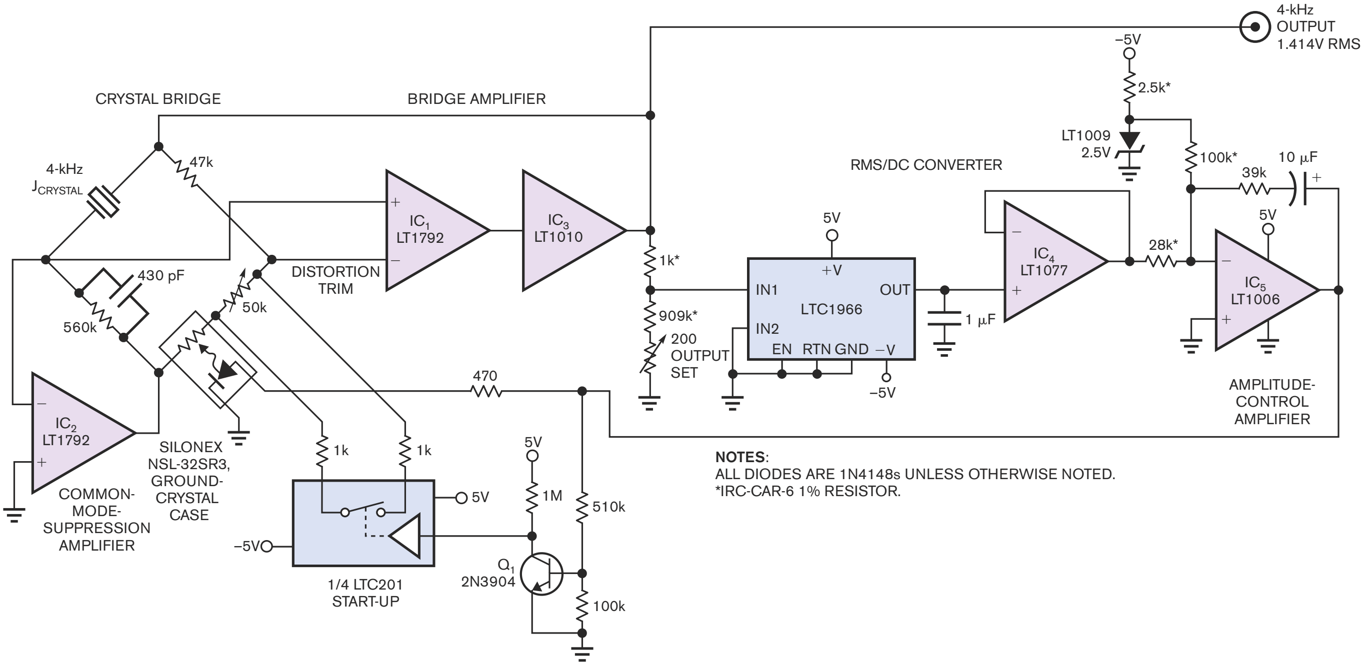

Figure 13 This quartz-stabilized sine-wave-output-ac reference has 0.1% long-term amplitude stability. The frequency accuracy is 0.01% with less-than-30-ppm distortion. The positive feedback around IC_1 causes oscillation at the crystal's resonant frequency. Amplifier IC_5 acts on the rms-amplitude output of IC_4 to supply a negative feedback to IC_1 through the bridge network that stabilizes the rms-output amplitude. The optocoupler minimizes feedback-induced distortion. Switch Q_1 closes during start-up, which ensures the rapid build up of oscillations.

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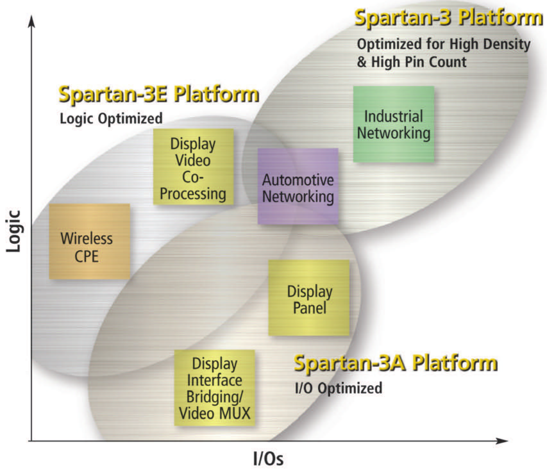

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The Ultimate Low-Cost Applications Platform feeds back to gain-control amplifier IC$_5$, which compares the rms value with a variable portion of the 5.1V zener potential. IC$_5$'s output sets IC$_2$'s gain through the 3-kΩ resistor, completing a control loop to stabilize noise-rms-output amplitude. The RC components in IC$_5$'s local feedback path stabilize this loop. You can vary the output amplitude using the 10-kΩ potentiometer; a switch permits external voltage control. Q$_1$ and associated components, a soft-start circuit, prevent output overshoot at power turn-on. **Figure 16** shows circuit-output noise in the 10-kHz filter position; **Figure 17**'s spectral plot reveals essentially flat rms-noise amplitude over a 500-kHz bandwidth.

RMS-AMPLITUDE-STABILIZED LEVEL CONTROLLER

Figure 18 borrows the previous circuit's gain-control loop to stabilize the rms amplitude of an arbitrary input waveform. You apply the unregulated input to variable-gain amplifier IC$_1$-IC$_2$ which feeds IC$_3$. DC coupling at IC$_1$-IC$_2$ permits passage of low-frequency inputs. An rms/dc converter, comprising IC$_4$ and IC$_6$, takes IC$_3$'s output, which feeds IC$_5$'s gain-control amplifier. IC$_5$ compares the rms value with a variable reference and biases IC$_1$,

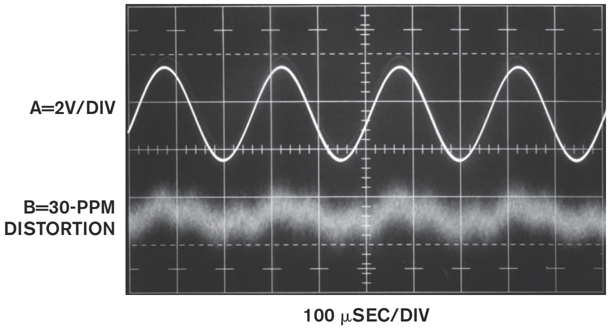
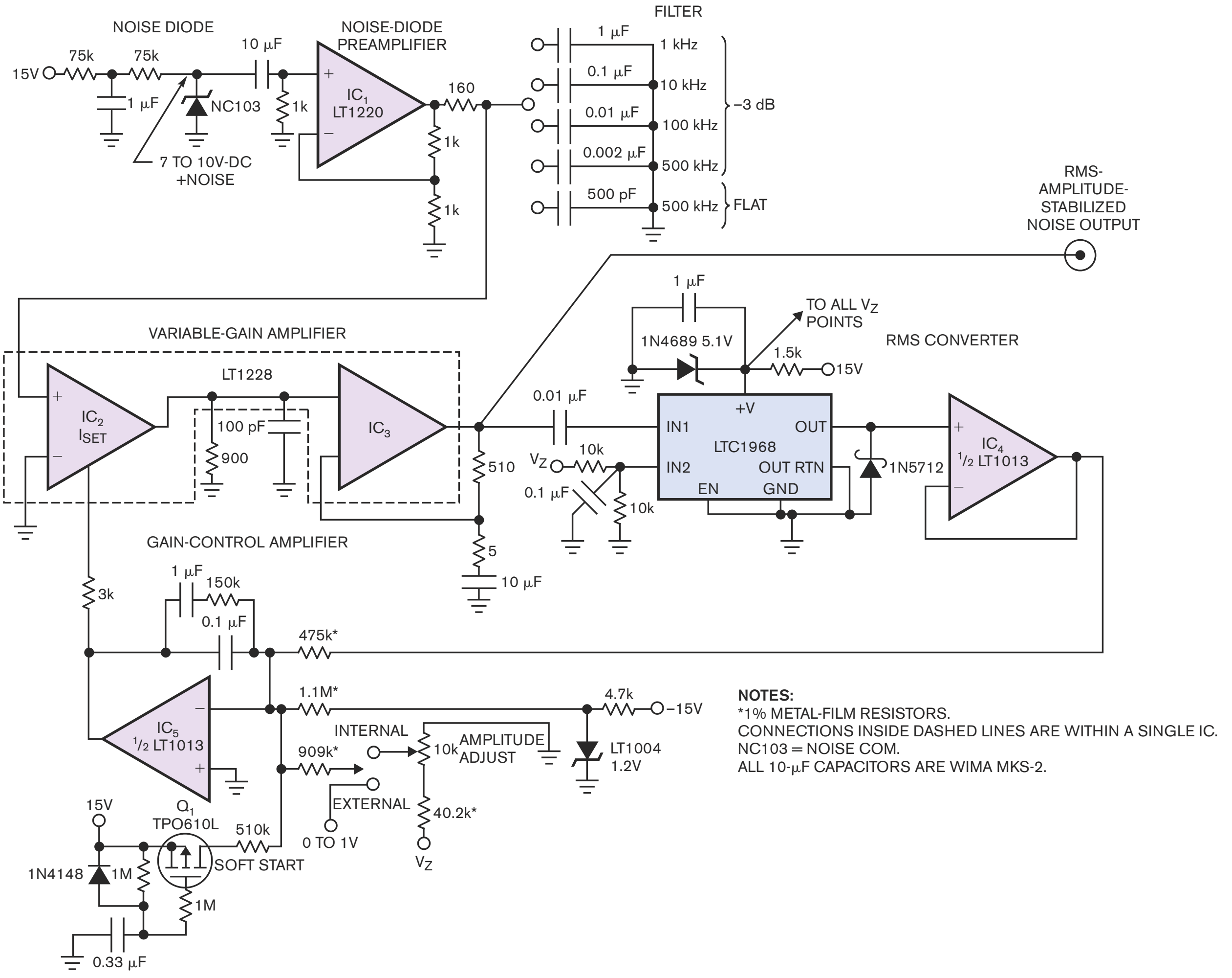


Figure 14 Trace A shows the 1.414V-rms (2V peak) reference output from IC$_3$. Trace B shows the 30-ppm distortion in the output. The distortion's constituents include noise, fundamental-related residue, and second-harmonic components.



NOTES:
*1% METAL-FILM RESISTORS.
CONNECTIONS INSIDE DASHED LINES ARE WITHIN A SINGLE IC.
NC103 = NOISE COM.
ALL 10-μF CAPACITORS ARE WIMA MKS-2.

Figure 15 This circuit creates a random-noise generator with rms-leveled output. IC$_1$ filters and amplifies zener-diode noise. The output of the variable-gain amplifier converts to rms. The rms output feeds back to gain-control amplifier IC$_5$, which closes the loop to the variable-gain amplifier. A potentiometer or external input to IC$_5$ allows you to set the noise output to different values.

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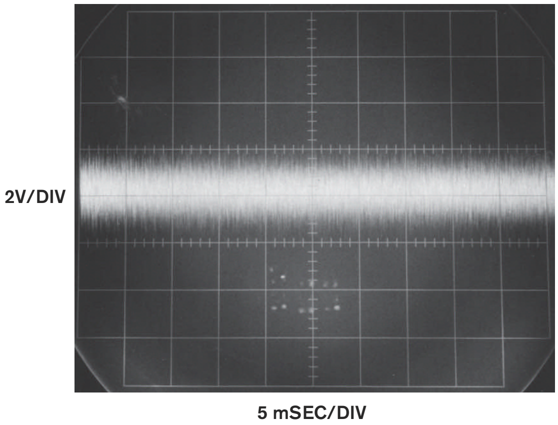


Figure 16 The output of the circuit in Figure 14 is in the 10-kHz filter position.

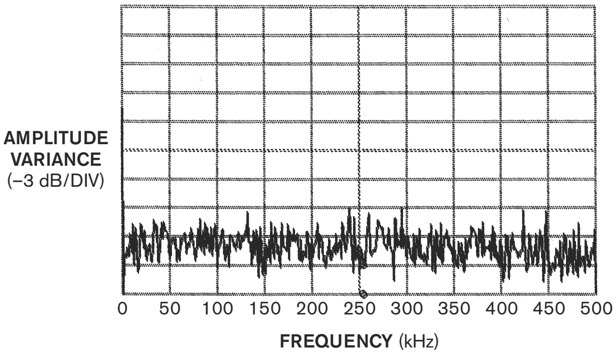
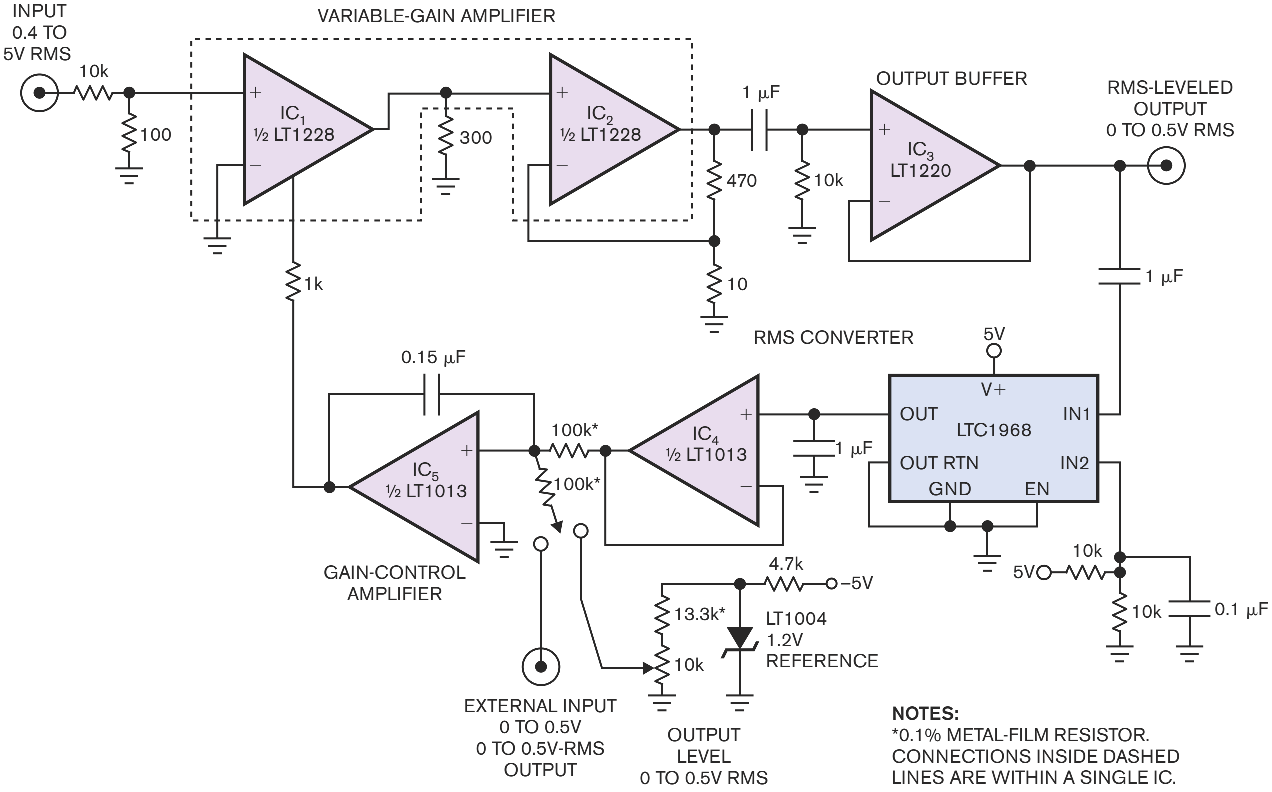


Figure 17 The amplitude over frequency for the random-noise generator is essentially flat to 500 kHz. The NC103 noise diode contributes to an even noise-spectrum distribution, and the rms converter and control loop stabilize the amplitude. The measurement sweep time is 2.8 minutes, and the resolution bandwidth is 100 Hz.

closing a gain-control loop. The 0.15-μF feedback capacitor stabilizes this loop, even for waveforms lower than 100 Hz. This feedback action maintains waveshape and stabilizes output-rms amplitude despite large variations in input amplitude. You can set the desired output level with the indicated potentiometer, or you can switch in an external control voltage.

Figure 19 shows output response (Trace B) to abrupt reference-level-setpoint changes (Trace A). The output settles within 60 msec for ascending and descending transitions. You can achieve faster response by decreasing IC_5's compensation capacitor, but the circuit would then be unable to process low-frequency waveforms. Similar considerations apply to **Figure**



NOTES:
*0.1% METAL-FILM RESISTOR.
CONNECTIONS INSIDE DASHED
LINES ARE WITHIN A SINGLE IC.

Figure 18 This rms-amplitude level-control circuit uses the gain-control loop of Figure 15. The amplifiers IC_1, IC_2, and IC_3 provide a variable-gain capability to the input section. The rms converter, IC_6, feeds back to the gain-control amplifier, IC_5, which closes the amplitude-stabilization loop. The variable-reference voltage permits a settable calibrated rms output that is amplitude-independent of the input waveshape.

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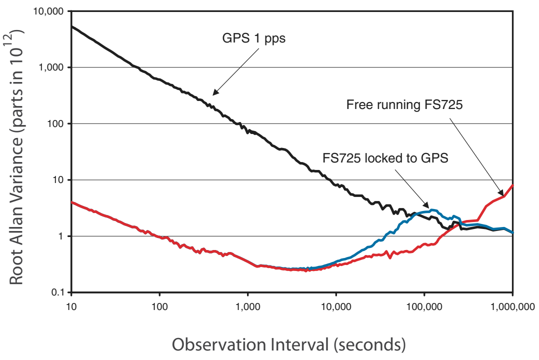
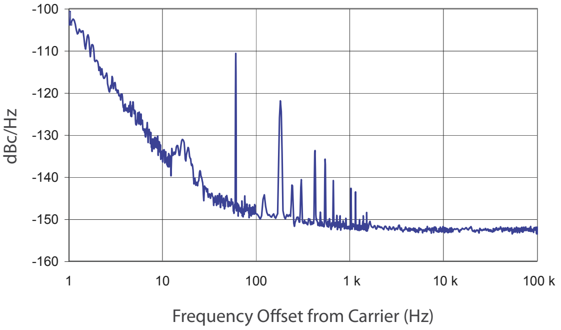


FS725 Single Sideband Phase Noise



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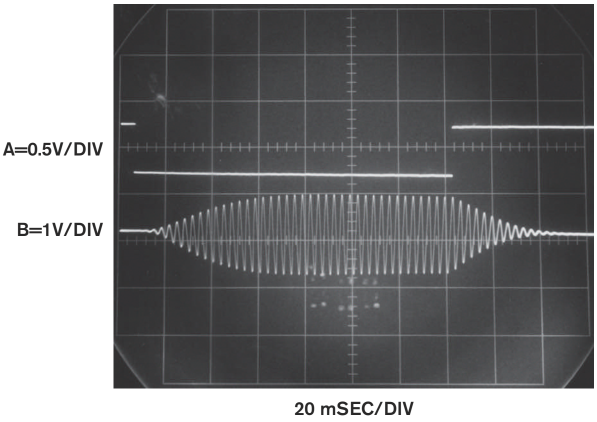

Figure 19 An abrupt change in the reference (Trace A) causes an amplitude-level-control response (Trace B). IC_5's compensation capacitor sets the settling time. This capacitor must be large enough to stabilize the loop at the lowest expected signal-input frequency.

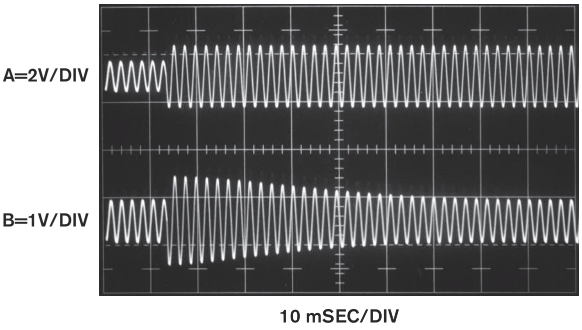

Figure 20 The amplitude-level-control output (Trace B) reacts to a step change in the input signal (Trace A). The slow loop compensation allows the overshoot, but the output settles cleanly.

20's response to an input-waveform step change. Trace A is the circuit's input, and Trace B is its output. The output settles in 60 msec due to IC_5's compensation. Reducing compensation value speeds response at the expense of low-frequency-waveform processing capability. Specifications include 0.1% output-amplitude stability for inputs of 0.4 to 5V rms, 1% set-point accuracy, 0.1- to 500-kHz passband, and 0.1% stability for 20% power-supply deviation.EDN

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AUTHOR’S BIOGRAPHY

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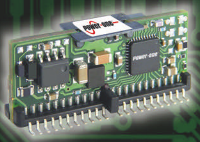

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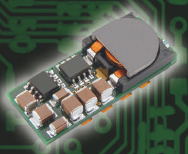

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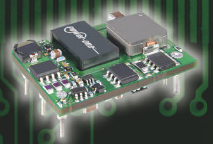

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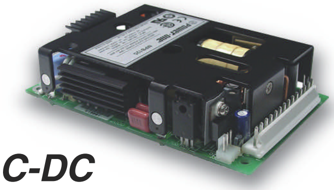

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Maximizing EOS and ESD immunity in high-performance serial buses

PROTECTING PRODUCTS FROM ELECTROSTATIC HAZARDS MAY SEEM TO INVOLVE BLACK MAGIC, BUT IT DOESN'T. A LAYERED STRATEGY OF DEFENDING AGAINST THE HAZARDS MAXIMIZES PRODUCTS' IMMUNITY AND MINIMIZES THE IMPACT ON PART COSTS AND PROJECT SCHEDULES.

EOS (electrical overstress) and ESD (electrostatic discharge) are the main causes of failures in semiconductors. Although EOS often takes the blame, ESD may sometimes accompany EOS. Did the assembly machinery zap the part? Did the handling procedures take the proper ESD precautions? Did the test equipment do something to the part? Or did the end user zap the part while crawling on a rug to reach a connector in back of a computer so he could plug in a cable? Figuring out the cause of device failures can present significant challenges. Eliminating the detective work by avoiding the failures is the most cost-effective approach. This article shows how to make pc boards as tolerant as possible of ESD and EOS.

ESD is a high-voltage external event that can get into your product and destroy the silicon. Typically, the discharges are common-mode-type events, which can result from many things, including insulation failures that you can detect only by careful scanning with an electronic microscope, sneak paths through internal protection diodes, and short circuits that enable conduction from a power rail to melt holes in the device. Because of their multiple causes, EOS problems don't yield to a single mitigation approach. EOS prevention is much like the defend-in-depth philosophy of medieval-castle builders: First, keep the ESD energy from getting in. (Keep the enemy out!) Second, dissipate the energy that does get in. (Make life hard for an enemy who gets through the first gate.) Third, make the silicon as resistant as possible to energy that does get in. (Put armor on your soldiers.)

The following recommendations are for high-speed serial buses, such as FireWire, USB, and, with extra care, PCIe (Peripheral Component Interconnect Express). Note that any hole in the chassis serves as an entry point for ESD. A high-speed serial bus may not be the problem. In fact, it may be the solution. By combining many outside connections, a single serial-bus connection can eliminate entry points for ESD (making it necessary to defend only one gate to the castle).

KEEP THE ENEMY OUT!

First, if possible, do not let ESD energy get to the silicon. The best way to accomplish this objective is with a Faraday cage. Ideally, a continuous conducting surface—typically, chassis ground—completely surrounds the internal electronics and connects to the green wire or earth ground. A good example of this approach is a PC's metal-tower case, a conducting enclosure that surrounds all the internal electronics. However, the high-speed serial bus requires a hole in that continuous surface to mount the connector to allow the electrical signals to enter. Well-designed serial buses have an overall external shield around the signal conductors and a metal shield on the pc-board connector. If a low-impedance connection connects the overall shield to the pc-board-connector shield and if a

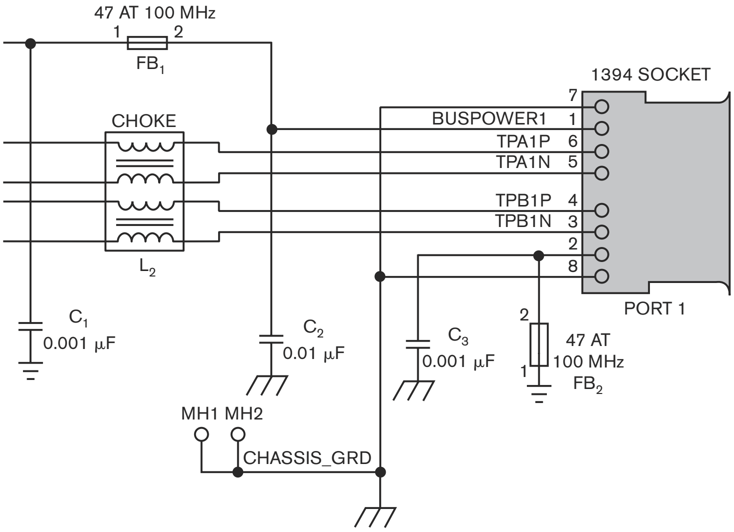

Figure 1 Carefully selected and located ferrite beads and capacitors as well as careful connector mounting maximize the immunity of the IEEE 1394 FireWire bus to electrostatic damage.

low-impedance connection ties the pc-board connector to the chassis ground, these connections form an almost-continuous conducting surface from one machine's metal enclosure, through the connector to the cable shield, and through to the mating connector to the connected machine's enclosure. The use of the word "almost" relates to the hole in the metal box from which the connector protrudes. This air gap can allow ESD energy in. Luckily, some devices use spring action to make contact from the connector shell to the enclosure's conducting surface. A vertical diagonal tang in these devices contacts the enclosure through which the connector protrudes, and a similar but horizontal tang contacts the pc-board connector, connects to the board's chassis ground, or both.

This construction mitigates both ESD and EMI (electromagnetic interference) by providing a short connection to the chassis ground from the connector shell and reducing the length of the slot antenna around the connector where it protrudes through the enclosure. Think of this arrangement as the wall around the castle. As long as the wall (Faraday cage) holds and nothing breaches the gates (connector holes), the people (silicon devices) inside are relatively safe.

If a product has no conducting enclosure, you have a couple of options: Try to dissipate the energy that gets in (that is, make life difficult for your enemy), or dump the ESD energy into the biggest bulk conductor available to let it bleed away over time. The disadvantage of dumping to the biggest bulk conductor is that doing so sends the ESD voltage everywhere that the conductor goes, giving it the opportunity to arc to other conductors or silicon devices. Also, the electric field can disrupt other silicon devices. If you can minimize these undesired possibilities by design, dumping to the biggest bulk conductor can be a good option.

MAKING LIFE DIFFICULT

Even if the enclosure is conductive, sneaky ESD can find ways inside. This insidious quality is the reason for in-depth defense. The goal of the second layer is to dissipate the energy that gets inside—that is, to make life difficult for any of the enemies who get past the first gate. You can think of the second layer as a lethal zone between the castle's external gate and the secondary gate. In castles, there was typically a hallway between these two gates with arrow slits in the walls to create a site for crossfire. In this hallway, defenders applied boiling oil to the invaders. Any enemy that got through the first gate (Faraday cage) had to survive this lethal zone before attempting to breach the second gate. The electronic world is slightly less dramatic. The goal is to dissipate as much energy as practical to minimize what reaches the silicon.

For FireWire, USB, and the cabled version of PCIe, a pair of conductors supplies dc cable power and provides a cable-power-return path. You can heavily filter these conductors to prevent ESD from getting to the silicon. With a few modifications, these conductors can also prevent EMI from escaping. Assume that the designer has shorted the connector's conducting shell to chassis ground with the previously described spring mechanism. Next, look at the power connection. For higher frequency ESD, you can place a capacitor to chassis ground as close as possible to the connector on both the power and the ground connections (C_1 and C_2 in **Figure 1**). However, the IEC (International Electrotechnical Commission) ESD-testing definition uses a 150-pF (C) capacitor charged to the test voltage (V). Because the total charge (Q) stays the same, to reduce this voltage below the capacitor voltage rating (50V), the protection-capacitor value must be approximately 0.033 μF (C=Q/V; therefore, V=Q/C). A 0.01-μF capacitor works in this application at 2-kV testing levels. You must use a high enough voltage capacitor, protect the capacitor with voltage clamps (such as zener diodes), or replace it with a high-voltage TVS (transient-voltage-suppressor) device. Because these connections are for power and ground, placing a large capacitor across them is not a problem.

Figure 1's circuit uses nonpolarized capacitors. Unfortunately, both of these examples' capacitor value is rather low. This approach allows a lower impedance path to dump ESD energy to chassis ground. Although it does not capture all of the energy, it captures enough to help. Relative to that of other routes for the energy, the impedance of the capacitor determines the amount of energy delivered to the capacitor and leads to the next protective element, a ferrite bead,

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FB_1, in series with the power connection. The ferrite presents a resistance to signals at high frequencies. At these higher frequencies, the bead exhibits higher impedance than that of the capacitor. The high-frequency edges are ESD's most damaging components. This combination of capacitor and ferrite aids in eliminating these edges.

With a small addition, this circuit becomes an effective EMI filter. The EMI filter is the converse of the ESD filter. The ESD filter tries to keep energy out, and the EMI filter tries to keep energy in. For EMI, the capacitor, C_3, next to the ferrite bead connects to the same ground as the transceiver, not to chassis ground. The idea is to return energy to its source, the transceiver chip. On the schematic, this arrangement now looks like a classic pi filter with the capacitors forming the legs and the ferrite at the top. Pay attention to the layout; it is important. To keep ESD out, the ESD capacitor should be as close as possible to the source of the ESD, the connector. But the EMI capacitor should be as close as possible to the source of the EMI, the transceiver chip. You should place the ferrite closer to whichever is the bigger problem. Place the bead close to the connector if ESD is the larger concern or close to the transceiver if EMI from the transceiver is more serious. If you lack enough information to decide, place the ferrite close to the connector. There, it will still keep EMI from the various sources from escaping the system and will do the most to prevent damage from ESD.

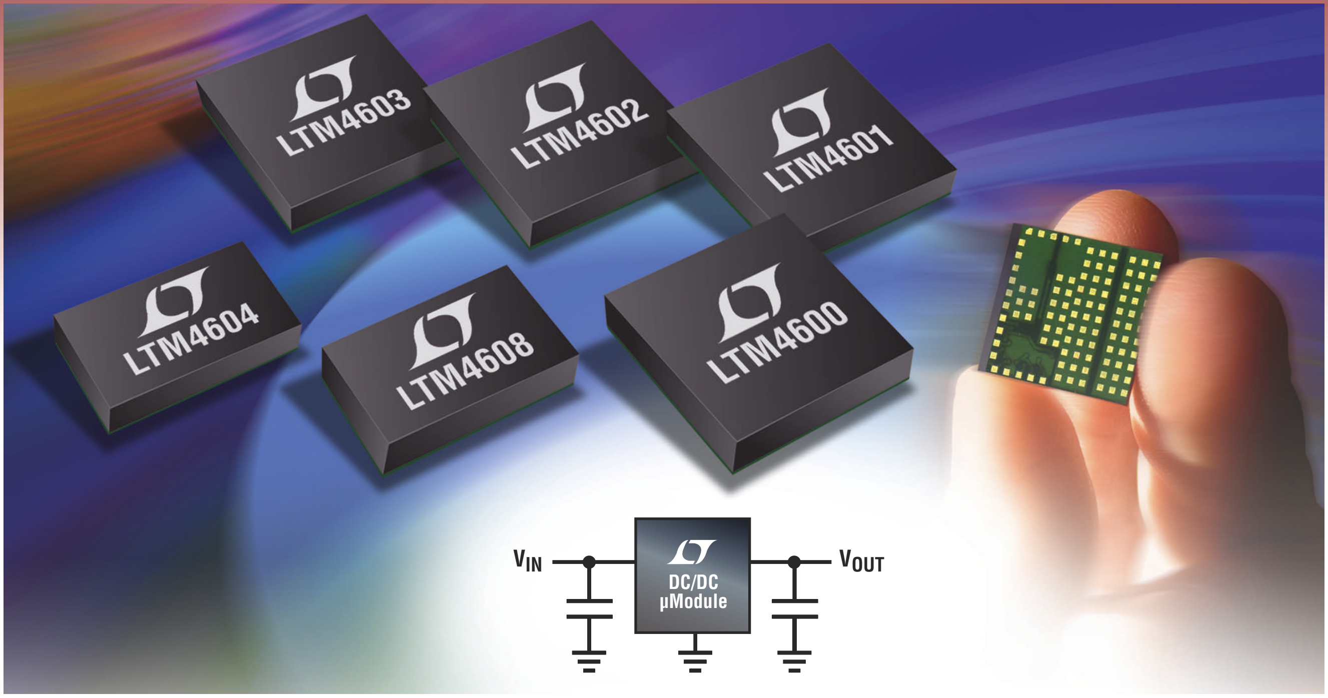
TRICKY GROUND CONNECTION

The ground connection is much trickier. Both FireWire and USB use common-mode signaling that requires a low-impedance return path—that is, the ground-return path through the cable's ground wire. For this reason, don't place a ferrite bead in series with the ground wire unless you have no other way to meet the ESD/EMI requirements. If you must use a bead, you should test it extensively to ensure that it works. However, you can aid ESD suppression by connecting a capacitor from signal ground to chassis ground as close as possible to the connector. This capacitor produces a current divider, and most of the current passes through the signal-to-ground connection. Some goes through the capacitor to chassis ground, however—with luck, enough to make a difference.

Trickiest are the high-speed signal lines, which you must treat equally. Anything you do to one of the lines you should do to both lines of the differential pair. The best approach is usually a common-mode choke for the technology you are using. The common-mode choke presents a high impedance to signals common to both conductors and lets differential signals pass. This approach works well for both ESD and EMI because both are typically common-mode phenomena. Again, component placement involves trade-offs. Placing the choke near the connector has the greatest effect on ESD. A position near the transceiver does the most to mitigate transceiver EMI. For the same reasons as those for ferrites, place the choke near the connector unless transceiver EMI is the dominant reason for adding the choke. For FireWire with two differential pairs, a single device with a common core uses less pc-board area. However, using a separate choke for each pair reduces crosstalk between the two pairs, which is often a good reason to use separate chokes despite the pc-board-area penalty.

You should take several issues into account and exercise caution concerning them. First, do not put capacitors on the high-speed, twisted-pair signal lines. In all cases, the frequencies present will cause any capacitance greater than a few picofarads to present signal-integrity problems. Although the product under test might at first seem to work, the bit-error rate can be high. Also, do not use common-mode chokes except those explicitly designed for the technology you are using. FireWire Version A (IEEE 1394a) uses a common-mode-signaling mechanism to determine the speed at which it can transfer packets. If a common-mode choke on the signal lines does not pass this common-mode signal, the higher speed packets will fail, even though the 98.304-Mbps packets work.

You also should avoid using a two-sided board. At the frequencies at which these serial buses operate, the loop impedance, which includes the outgoing-signal path plus ground-return path, determines the signal integrity and the amount of radiated EMI. Having a solid ground plane underneath traces and not using vias on these traces greatly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eases the layout job. Introducing vias hurts signal integrity, and you must then worry about connecting image planes to minimize the signal-path loop area; the layout quickly becomes excessively complex. Use a four-layer board with a solid ground plane underneath the twisted-pair signal lines from transceiver to connector pins. Use a solid flood for a chassis-ground plane that connects to the connector shell and provides a connection point for the components that connect to chassis ground. When laying out such a board, give higher priority to placing a solid signal-ground plane under the complete length of the signal lines than to achieving a simple shape for the chassis-ground flood.

ARMOR YOUR SOLDIERS

If ESD gets past the dissipation defenses, the situation is as if enemy soldiers have gotten into the keep; now you must fight. You must protect the devices from any energy that gets beyond the defenses you have set up. All silicon devices have built-in ESD protection of some sort; check the data sheet. But, almost always, you can do more on the pc board. Your goal is to keep anything from upsetting the silicon's function. The first things to check are any reset pins. You must protect them from accidentally changing state. If the reset pin's threshold is referenced to ground, as most are, place a capacitor from the reset pin to ground. The capacitor helps to keep the reset pin from changing state during a ground-bounce event. In this case, an event changes the level of the ground reference; if it changes too much, the silicon can execute a reset. During brief ground bounces, a capacitor from the reset pin to ground helps to hold constant the nominal voltage between the pin and ground. During longer events, the capacitor's charge drains off, allowing the voltage to change, maybe to the point of exceeding the threshold. For this reason, make the value of this capacitor as large as possible. If the reset pin is almost a dc signal, put a greater-than-1-µF capacitor on it. Use a lower value capacitor if it places too much of a load on the driving signal or too greatly limits the frequency, but, in this case, bigger is nearly always better. This same reasoning applies to all of the inputs that could be disruptive to the silicon. In the case of FireWire physical layers, take special care with the reset and LPS (link-power-status) pins.

For other pins that could encounter an ESD strike, every little bit of resistance that you can add between the silicon and the ESD strike helps to protect the silicon. For example, placing a 10Ω resistor in series with a signal as close as possible to the silicon without seriously affecting it increases the device's ESD tolerance. Adding these elements is like equipping your soldiers with armor. Knights in armor or chain mail are more formidable for combat than those in fabric clothing.

HOW MUCH DEFENSE?

Are all of these measures necessary? It depends. If you are building only a few boards, by all means spend the extra money and time to make them as robust as possible. When you design a high-speed serial bus into a product, the money and time you spend on design and parts are two of the best risk trade-offs you can make. The cost of an extra run through the EMI and ESD ranges is more than that of the components and design time to put them on the pc board and build a hundred or so boards. It is also well worth the cost if the schedule is critical and a second or third run through the ESD and EMI ranges would cause you to miss a critical window. When board volumes are higher, the balance can change. Building thousands of boards and saving a dollar per board would pay for several runs through the ESD and EMI ranges. Remember, though, that it costs little to design a board to accommodate many protective items that may later prove superfluous. To manage the costs, if a component turns out to be unnecessary, you can remove it from the bill-of-materials cost or replace it with an inexpensive, 0Ω resistor. This exercise constitutes a classic balancing of risk, and each designer must do it.**EDN**

AUTHOR'S BIOGRAPHY

As a senior member of the technical staff at Texas Instruments (Dallas), Burke Henehan defines audio amplifiers for mobile devices. He holds a master's degree in systems engineering from Texas Tech University (Lubbock, TX) and a bachelor's degree in electrical engineering from South Dakota School of Mines and Technology (Rapid City, SD). You can reach him at bh055@yahoo.com.

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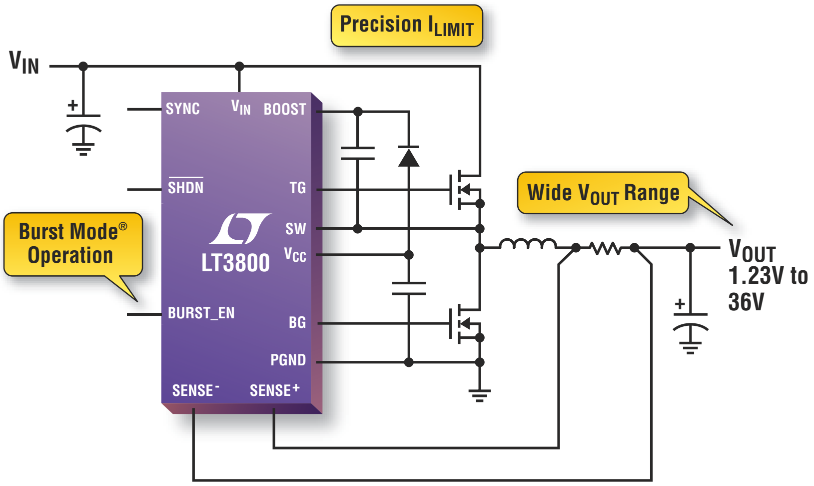

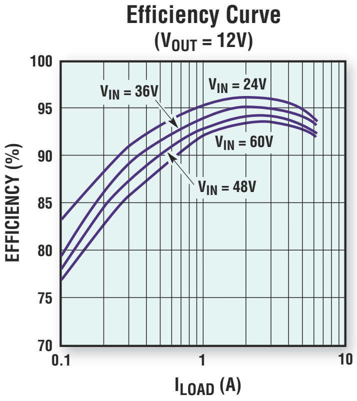

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Switchmode Controllers							
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LT3724				80	-	200	Fixed 200kHz Operation
LTC®3824			0.8V to V_{IN}	40	200 to 600	200 to 600	100% Duty Cycle, Low Dropout
LT3800	20	4 to 60	1.23V to 36V	80	-	200	Synchronous Drivers
LT3845				120	100 to 600	100 to 500	
Switchmode Monolithics							
LT3437	0.4	3.3 to 80	1.25 to 0.9xV_{IN}	100	240 to 700	200	Ultrawide V_{IN}
LT1976	1.3	3.3 to 60	1.2 to 0.9xV_{IN}	100	230 to 700		
LT3434	2.5	3.3 to 60	1.25 to 0.9xV_{IN}	100	230 to 700		

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DESIGN NOTES

Versatile Voltage Monitors Simplify Detection of Overvoltage and Undervoltage Faults – Design Note 408

Scott Jackson

Introduction

Many modern electronic systems have strict power supply operating ranges—requiring accurate monitoring of each supply. Some systems must know that all supplies are present and stable before startup and some must know if the supplies deviate from safe operating conditions.

The LTC®2912, LTC2913, and LTC2914 supervisors respectively monitor single, dual, and quad power supplies for undervoltage and overvoltage with tight 1.5% threshold accuracy over temperature. All monitors in the multiple-monitor devices share a common undervoltage output and a common overvoltage output with a timeout period that is adjustable or disabled. Each monitor has input glitch rejection to ensure reliable reset operation without false or noisy triggering.

Each part has at least two options: one with capability to latch the overvoltage output and one with capability to externally disable both outputs. The LTC2912 has a third option with latching capability and a non-inverted overvoltage output. Each part has an internal 6.5V shunt regulator allowing the device to be used in a system with any supply level.

Basic Operation

Figure 1 shows a typical application for the LTC2914. Each monitored input is compared to a 0.5V threshold. Any channel can be configured to monitor both undervoltage and overvoltage conditions using a 3-resistor divider. When monitoring a positive voltage, the VH input of the channel is connected to the high-side tap of the resistive divider and triggers an undervoltage condition while the VL input is connected to the low-side tap of the resistive divider and triggers an overvoltage condition. When an

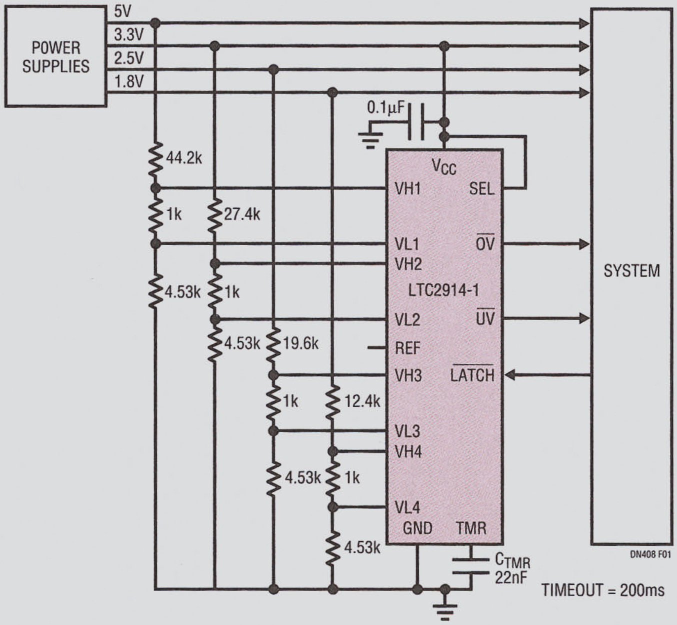

Figure 1. Quad UV/OV Supply Monitor

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undervoltage condition is detected, the $\overline{UV}$ output asserts low.

Once all undervoltage conditions clear, the $\overline{UV}$ output remains asserted until a timeout period has elapsed. This timeout period is set by a capacitor between the TMR and GND pins. The timeout period can be disabled by tying the TMR pin to V_{CC}. Figure 2 shows the timeout period versus TMR capacitance. The $\overline{OV}$ output behaves in a similar manner. On parts with latching capability, the $\overline{OV}$ output latches when asserted until cleared by the $\overline{LATCH}$ pin. Holding the $\overline{LATCH}$ pin high bypasses the overvoltage latch.

Minimum Fault Length Monitor

The LTC2912-3 can be used to detect an undervoltage condition with a minimum duration by using the VL input and the non-inverted OV output. For example, an automobile system may need to monitor the 12V power supply during a power up condition. During the initial cranking of the automobile, the power supply droops. If the supply droop exists for an extended period, the system may need to disconnect various circuits from the supply for protection or disconnect circuits to reduce the load. This is accomplished by the circuit shown in Figure 3.

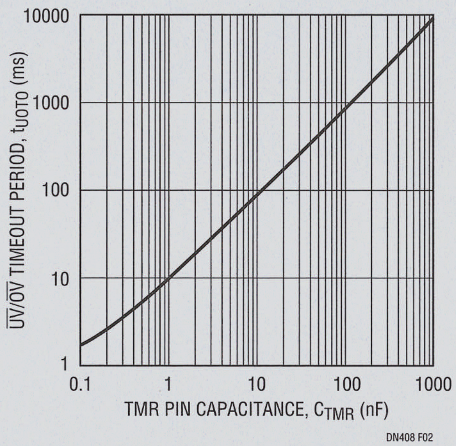

Figure 2. Timeout Period vs Capacitance

The timeout function of the LTC2912 typically starts when a fault clears. However, because the VL input is used in this case to monitor an undervoltage instead of an overvoltage, the timeout function occurs at the beginning of an undervoltage condition and the OV output remains high until the period has elapsed. If the fault still exists when this timeout period elapses, the OV output ($\overline{FAULT}$) pulls low until the fault clears. Choosing a 0.47µF timing capacitor produces a 4.1s timeout delay. Therefore, any supply droop lower than 9.6V and longer than 4.1s asserts FAULT. Figure 4 shows the resulting waveform of a supply fault condition of 9V for 5 seconds.

Conclusion

The LTC2912, LTC2913, and LTC2914 simplify power supply monitoring of any voltage level by offering superior performance and flexibility. Only a few resistors are needed to configure monitoring of multiple voltages for both undervoltage and overvoltage conditions. The LTC2914 offers these features in a 16-lead SSOP and 16-lead (5mm × 3mm) DFN package, the LTC2913 in a 10-lead MSOP and 10-lead (3mm × 3mm) DFN package, and the LTC2912 in a tiny 8-lead ThinSOT™ and 8-lead (3mm × 2mm) DFN package.

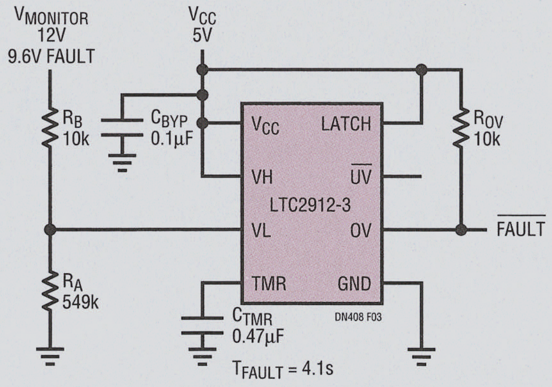

Figure 3. Fault Detection Circuit for a 4.1s Undervoltage Condition

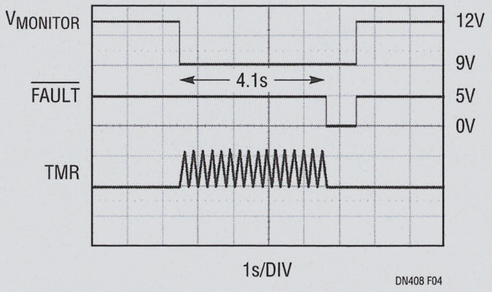

Figure 4. Fault Detection Waveform of a 4.1s Undervoltage Condition

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Simple circuit allows long PWM soft starts

Robert N Buono, Aeolian Audio LLC, Bloomfield, NJ

Available from multiple sources, the UC384X family of current-mode, PWM (pulse-width-modulated) power-supply controllers offers good performance and has spawned a variety of similar ICs. All members of the UC384X family and its variants share a common characteristic—an internal voltage-error amplifier that provides a current-limited output. Designated as the COMP pin, the amplifier's output provides a convenient connection for applying compensation to ensure overall feedback-loop stability. In addition, the COMP pin allows attachment of shutdown and soft-start circuitry and serves as a convenient point for setting an external power switch's output-current-limit threshold.

Two of the COMP pin's characteristics enhance its versatility: First, the pin delivers limited output current, and, second, the pin's voltage is directly proportional to the current flowing through an external power switch. Both features also allow the pin to serve as a control port. For example, perhaps the most common application for the pin involves addition of a soft-start feature to a UC384X-based power-supply design.

In soft-start mode, an external power switch's output current and the power supply's output voltage ramp up at a rate controlled by, and proportional to, the voltage at the COMP pin. **Figure 1** shows a typical soft-start circuit's implementation comprising a small-signal PNP transistor, Q_1, connected to the COMP pin. An RC network, R_1 and C_{SS}, drives Q_1's base from IC_1's internally generated, 5V precision-reference source.

When the external power-supply voltage, V_{DD}, exceeds IC_1's internally preset UVLO (undervoltage-lockout) threshold, the 5V reference source switches on. The voltage on C_{SS} ramps upward toward 5V at a rate that the time constant, τ, of $R_1 \times C_{SS}$ determines in seconds. Given Q_1's emitter-follower configuration, Q_1 applies the COMP pin's voltage, which "follows" Q_1's base voltage, and the power supply's output current ramps up proportionally.

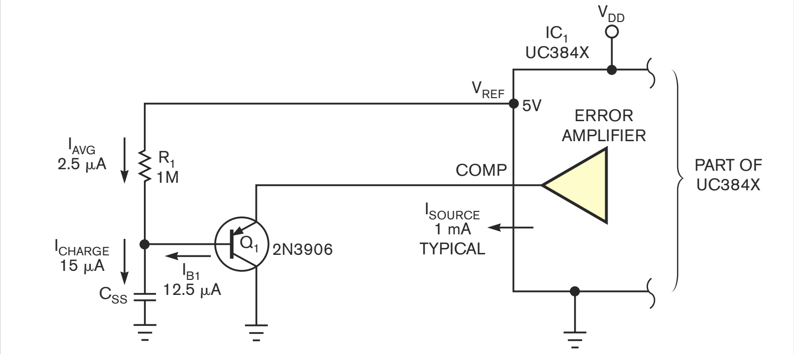

Figure 1 A single transistor, Q_1, implements a switching regulator's slow-start-up feature, but its base current introduces a timing error.

The simple circuit in **Figure 1** satisfies the requirements of many soft-start applications. To obtain longer soft starts, you can increase C_{SS} or increase R_1 to decrease C_{SS}'s charging current. However, increasing either component can cause problems. Depending on the construction of capacitor C_{SS}, its leakage current may be significant. Also, you can no longer ignore Q_1's base current. For example, a survey of PWM-control-IC designs shows that the COMP pin typically sources an output current of 1 mA. If Q_1, a 2N3906, provides a minimum beta of 80, Q_1's base draws a minimum current of 12.5 µA. The base current flows from the base pin of Q_1 and adds to C_{SS}'s charging current. If the circuit in **Figure 1** uses a 1-µF capacitor for C_{SS} and a 1-MΩ resistor for R_1, you would expect a nominal 1-second charging-time constant and an average charging-current flow of 2.5 µA through R_1. However, the charging current actually totals 15 µA—the sum of the 2.5-µA charging current plus Q_1's 12.5-µA base current, and the soft-start time falls considerably short of the nominal value.

As an alternative, the circuit of **Figure 2** better satisfies designs such as

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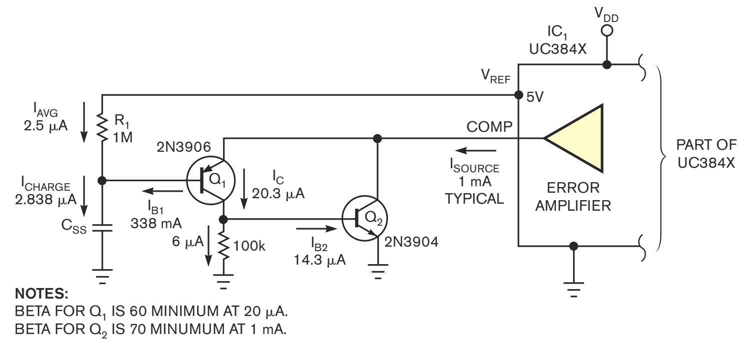
battery chargers that require a longer soft start or a more accurately timed soft-start ramp. Adding a second transistor to form a PNP-NPN compound transistor maintains the slow-start function. The circuit's composite current gain (beta) consists of the product of Q_1's and Q_2's current gains, or 70×60=4200, which greatly exceeds the single transistor's current gain of 60. The higher current gain reduces the charging current's base-current component to only 338 nA. **Figure 3** compares the responses of both circuits. The dark-green trace shows that the circuit of **Figure 2** produces the expected 1-second soft-start time interval, and the light-green trace illustrates **Figure 1**'s too-brief start-up time. Although the circuit of **Figure 2** yields a more accurate soft-start ramp, it also allows the use of smaller capacitors, such as multilayer ceramics, to reduce pc-board area and component cost.

Although a Darlington-connected transistor pair would also provide high current gain, its output transistor cannot saturate—a prerequisite for keeping the off-state voltage at IC_1's COMP pin below 1V. The PNP transistor, Q_1 in the PNP-NPN compound connection in **Figure 2** can saturate, and the NPN transistor, Q_2, maintains its voltage-controlled saturation voltage at significantly less than 1V over the circuit's operating-temperature range.**EDN**



NOTES:
BETA FOR Q_1 IS 60 MINIMUM AT 20 μA.
BETA FOR Q_2 IS 70 MINUMUM AT 1 mA.

Figure 2 Replacing Q_1 in Figure 1 with a PNP-NPN compound-transistor pair dramatically reduces the circuit's start-up-ramp-timing error.

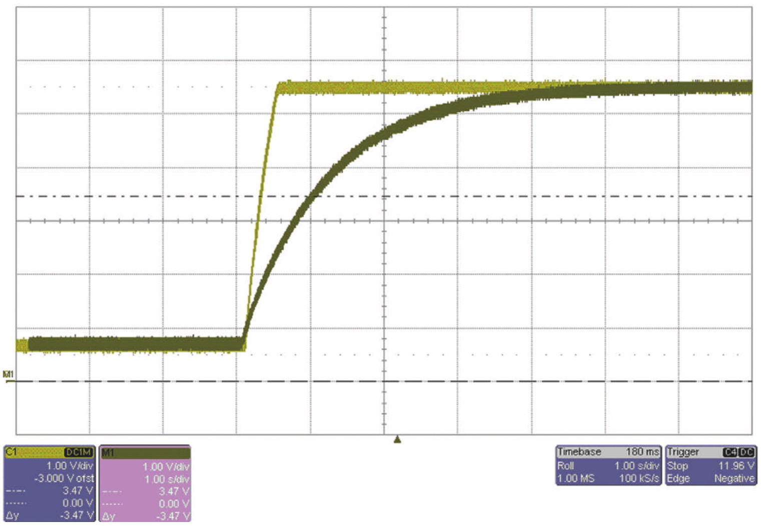


Figure 3 The dark-green trace shows that the circuit of Figure 2 produces the expected 1-second slow-start time interval, and the light-green trace illustrates Figure 1's too-brief start-up time. (The 1τ measurement equals 1 second.)

Open-door alarm prevents accidental defrosts

Tom Lyons Fisher, Juniata College, Huntingdon, PA

Laboratory refrigerators and freezers often contain very valuable materials. Some units include overtemperature alarms that typically don't sound until thawing has already damaged the units' contents or sound when no one is around to hear the warning. Rather than a power outage, the most frequent cause of thawing disasters involves a failure on someone's part to properly close the freezer's door. This Design Idea describes an alarm that provides a timely open-door warning that can prevent an expensive incident.

A decade ago, a designer would have based this circuit on a type-555 timer IC, but, today, a small microcontroller provides a less expensive approach. The alarm in **Figure 1** detects an open refrigerator or freezer door by means of a magnetic proximity switch that's available from Radio Shack (www.radioshack.com) as an intrusion-alarm-system component. The circuit allows the door to remain open for a software-selectable interval—in this instance, 20 seconds—before activating a piezoelectric buzzer that conserves battery power by sounding for only 1 second of every 5.

A low-dropout voltage regulator, IC_1, an STMicroelectronics (www.st.com) L4931CZ50, provides 5V regulated power for IC_2, a Microchip (www.micro

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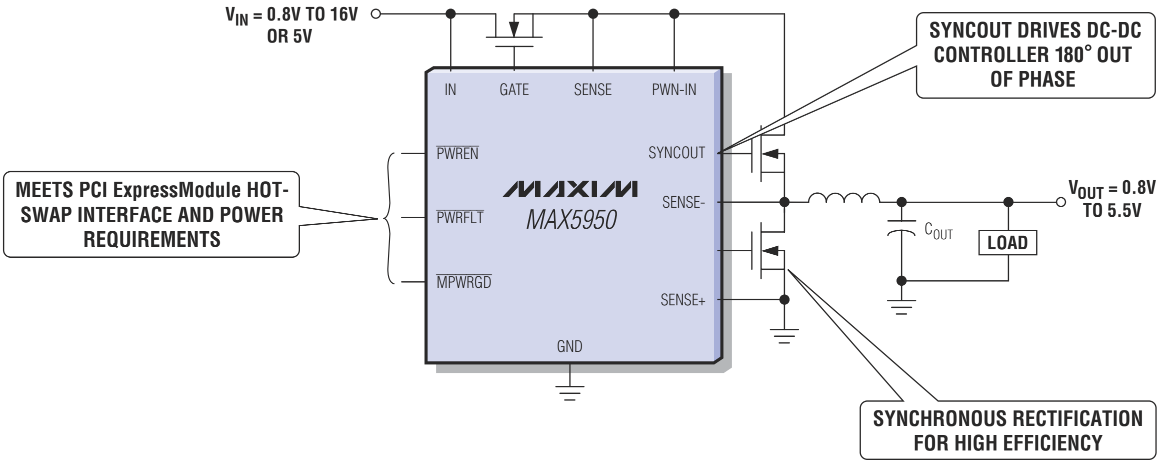

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MAX5951	No	32-TQFN	1.69

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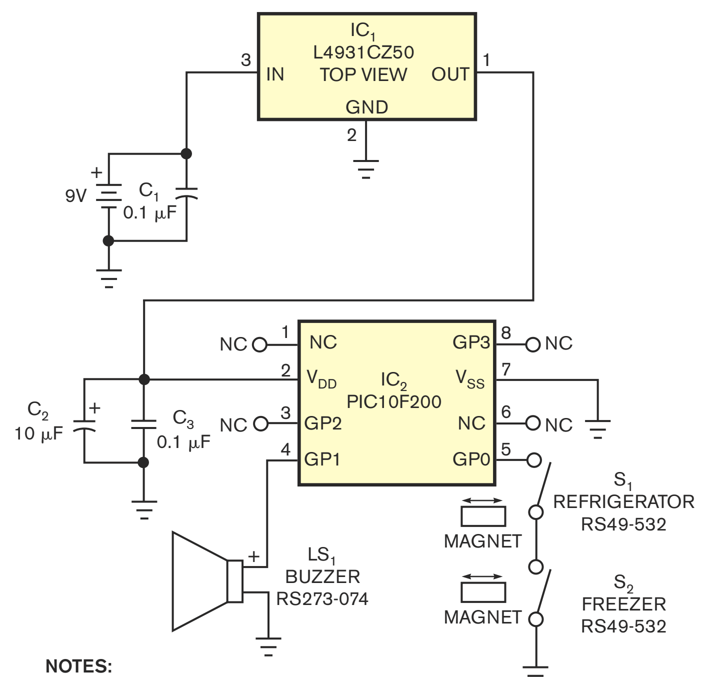
chip.com) PIC10F200. Because IC_2 "sleeps" between door openings and voltage regulator IC_1 consumes little quiescent current, the 9V alkaline battery that powers the circuit offers a projected life of approximately one month. When you activate the buzzer, it consumes approximately 2 mA, a drive current that's directly available from the microcontroller's output port. At this current level, only an uncased piezoelectric element provides a sufficiently loud warning. In high-noise environments, you can use a solid-state relay or a logic-level MOSFET to drive the buzzer directly from the 9V battery.

You can attach the normally open switches and their actuation magnets to the refrigerator or freezer using double-sided adhesive-foam tape. The switches are sensitive to magnet orientation and position, making it easy to find a mounting configuration that can detect a door that's open by as little as 2 mm. Source code for the microcontroller is available for downloading from the online version of this Design Idea at www.edn.com/070201di1.**EDN**



NOTES:
RS DESIGNATES A RADIO SHACK PART NUMBER.
S_1 AND S_2 ARE NORMALLY HELD CLOSED BY THEIR RESPECTIVE MAGNETS.

Figure 1 This circuit protects the contents of a laboratory freezer or refrigerator by sounding an alarm when a door opens.

LED drivers minimize power dissipation

Fons Janssen, Maxim Integrated Products Inc, Bilthoven, Netherlands

One option for driving high-brightness LEDs uses the standard stepdown buck converter (**Figure 1**). The sense resistor, R_S, generates a feedback voltage, V_{FB}, that sets the desired LED current, I_{LED}, according to the equation $R_S=V_{FB}/I_{LED}$. Unfortunately, most buck converters require a relatively high feedback

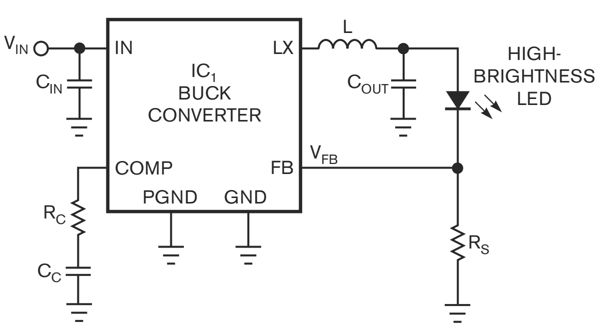


Figure 1 A generic buck converter, IC_1, provides constant-current drive for a high-brightness LED.

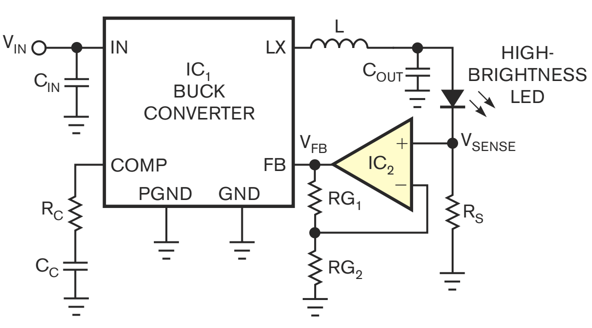


Figure 2 An op amp, IC_2, increases the LED-current error signal and reduces power dissipation in the sense resistor.

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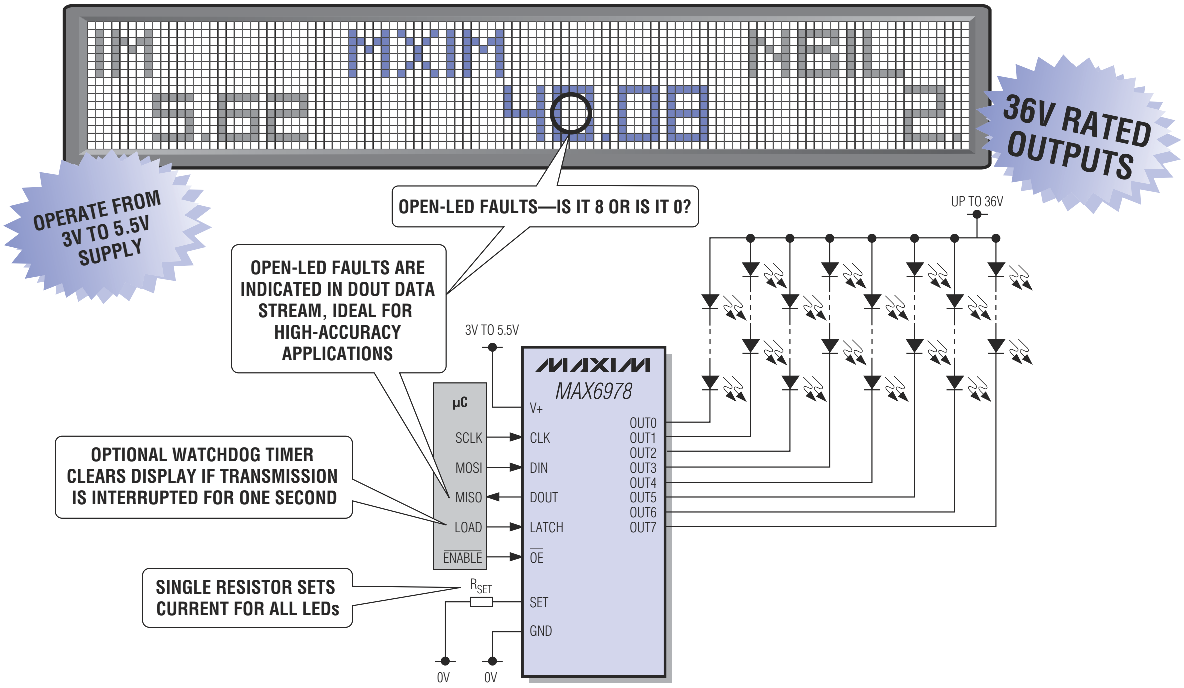

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SINGLE RESISTOR SETS CURRENT FOR ALL LEDs

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MAX6968	8	5.5V	55mA	—	—	-40°C to +125°C
MAX6977				Yes	—	
MAX6978				Yes	Yes	
MAX6970		36V		—	—	
MAX6981				Yes	—	
MAX6980				Yes	Yes	
MAX6969	16	5.5V		—	—	
MAX6979				Yes	Yes	
MAX6971		36V		—	—	
MAX6983				Yes	Yes	

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voltage on the order of 1V, which dissipates high power in the sense resistor ($P_{SENSE}=V_{FB}/I_{LED}$). Reducing the sense resistor's value and adding an op amp to boost the sensed voltage reduces the power penalty (**Figure 2**). In some cases, you can eliminate the op amp by using a stable reference voltage, which is available on some converter ICs, to pull up the sense voltage (**Figure 3**).

> THE VARIATION OF LED CURRENT AVERAGES APPROXIMATELY 5 mA OVER AN INPUT-VOLTAGE RANGE OF 4 TO 5.5V.

The switching converter, a Maxim (www.maxim-ic.com) MAX1951, requires a feedback voltage of 800 mV and provides a 2V reference voltage at the reference pin. Connecting R_1, a 50-kΩ resistor, between R_S and V_{FB}, and R_2, a 100-kΩ resistor, between the reference and the feedback pins shifts the operating point from 200 mV at R_S to 800 mV at the feedback pin:

$$V_{FB}=V_{REF}\frac{50k}{50k+100k}+V_{SENSE}\frac{100k}{50k+100k}=0.667V+{}^{2}/_{3}(V_{SENSE}).$$

Thus, for V_{SENSE}=0.2V, V=0.8V. For the cost of two inexpensive resistors, power dissipation in the sense resistor diminishes by a factor of four.

Using the Luxeon K2 LED from Lumileds (www.lumileds.com), power measurements on the circuits of **figures 1** and **3** illustrate how the feedback adjustment influences power that the LED driver delivers. Two graphs illustrate LED currents and voltages as a function of input voltage for a half-load of 400 mA (**Figure 4**) and a full load of 800 mA (**Figure 5**). As you would expect, the current regulation deteriorates at half-load. The variation of LED current averages approximately 5 mA over an input-voltage range of 4 to 5.5V and 1 mA for the circuit

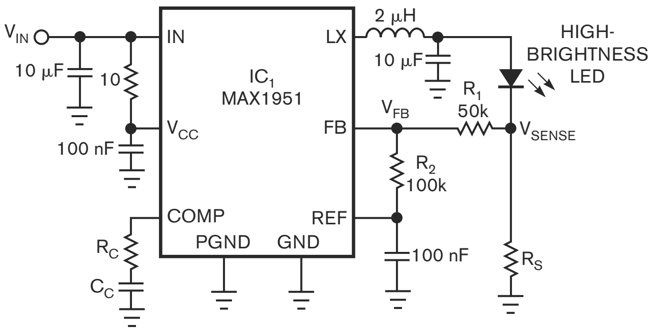

Figure 3 Adjusting the feedback signal improves the efficiency in this buck-converter driver for high-brightness LEDs.

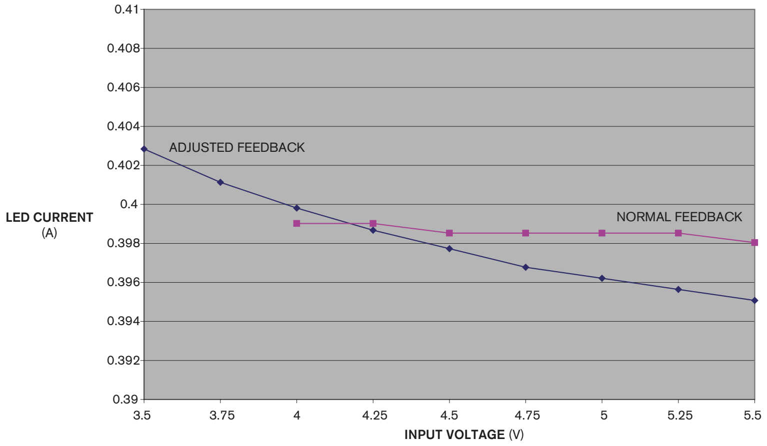

Figure 4 This graph shows LED current as a function of input voltage at half-load for the circuit of Figure 3.

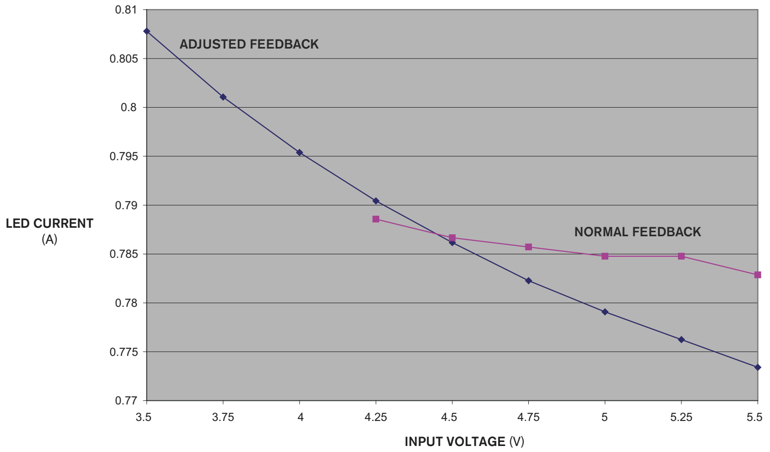

Figure 5 This graph shows LED current as a function of input voltage at full load for the circuit of Figure 3.

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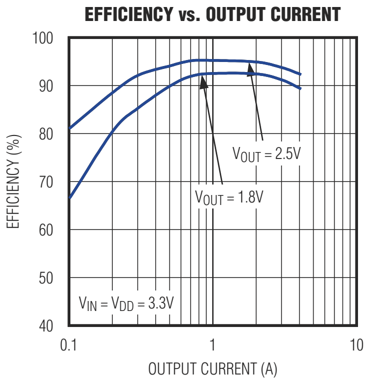

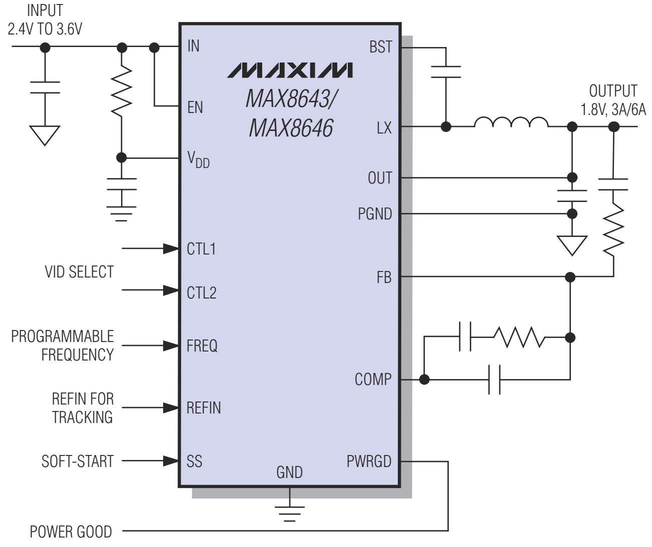

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with normal feedback. The input-voltage range, however, increases by more than 0.5V. Regulation also deteriorates for full load, and the variation increases to approximately 22 mA versus 6 mA for the circuit with normal feedback (**Figure 6**). Again, the adjusted-feedback circuit of **Figure 3** increases the input-voltage range.

You can define the improvement in efficiency, η, as follows:

$$\eta = \frac{V_{LED} \times I_{LED}}{V_{IN} \times I_{IN}}.$$

The buck converter's power-conversion efficiency and power dissipated in the sense resistor determine the circuit's efficiency. As **Figure 5** shows, the adjusted feedback of **Figure 3** increases the efficiency more than 10% at either half-load or full load. Assuming that the sense voltage doesn't change, efficiency improves for lower output-current loads because the sense resistor dissipates less power.**EDN**

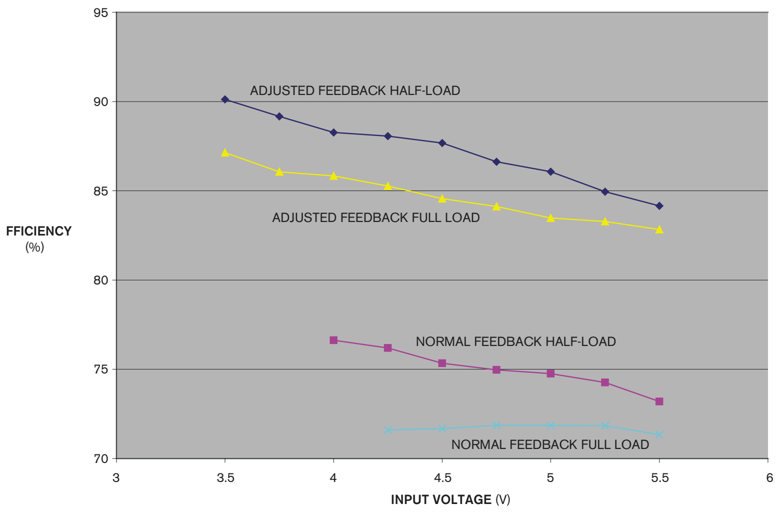

Figure 6 A comparison of a normal-feedback circuit (Figure 1) and an adjusted-feedback circuit (Figure 3) shows significant improvements in overall efficiency at half-loads and at full loads.

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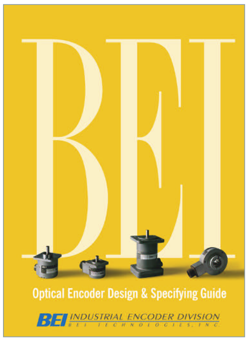

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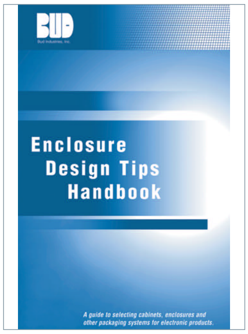

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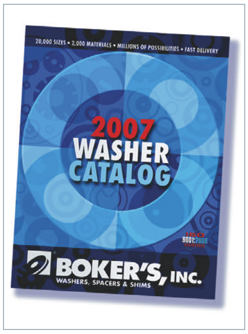

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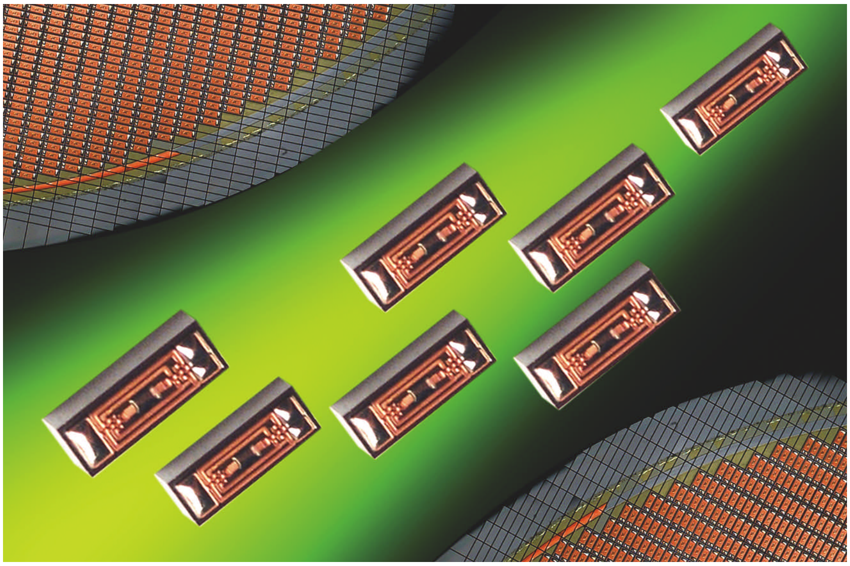

Thin-film RF inductor comes in miniature package

Based on thin-film-multilayer technology, the 0402 LGA (land-grid-array) inductor provides a high Q and tight tolerances with high current-handling capabilities and repeatability. The RF inductor features a 0.82- to 6.8-nH inductance range. LGA packaging suits the device for use in mobile-communication devices, satellite-TV receivers, GPS (global-positioning-system) units, and wireless LANs. Prices for the 0402 range from 10 to 30 cents.

AVX Corp, www.avx.com

Low-ESL MLCCs comes in a variety of sizes

Available in 0402, 0603, and 0805 case sizes, the low-ESL (equivalent-series-inductance) WK MLCC (multilayer-ceramic-capacitor) series comes in 0.47-, 4.7-, and 10-μF maximum-capacitance values, respectively. The 0402 package comes in a 4V voltage rating, the 0603 comes in 4 and 6.3V voltage ratings, and the 0805 comes in 6.3 and 16V voltage ratings. Measuring 1×0.5×0.3 mm, the WK series 0402 costs 15 cents. The WK series 0603 measures 1.6×0.8×0.8 mm and costs 20 cents. The WK series 0805 measures 2×1.25×0.85 mm and costs 30 cents.

Taiyo Yuden, www.yuden.us

Open-air resistor suits current sensing in automotive applications

This version of the vendor's open-air current-sense resistor has a higher power rating than conventional metal-element-resistive devices. The OARS-XP series includes a wider metal-alloy-resistive element, providing improved TCR (temperature coefficient of resistance) and thermal compliance. Features include a 2- to 50-mΩ resistance, ±1 and ±5% inductance tolerance, less than 10-nH inductance, and a −40 to +125°C operating temperature. Targeting automotive applications, the OARS-XP series costs 40 cents (1500).

IRC, www.irctt.com

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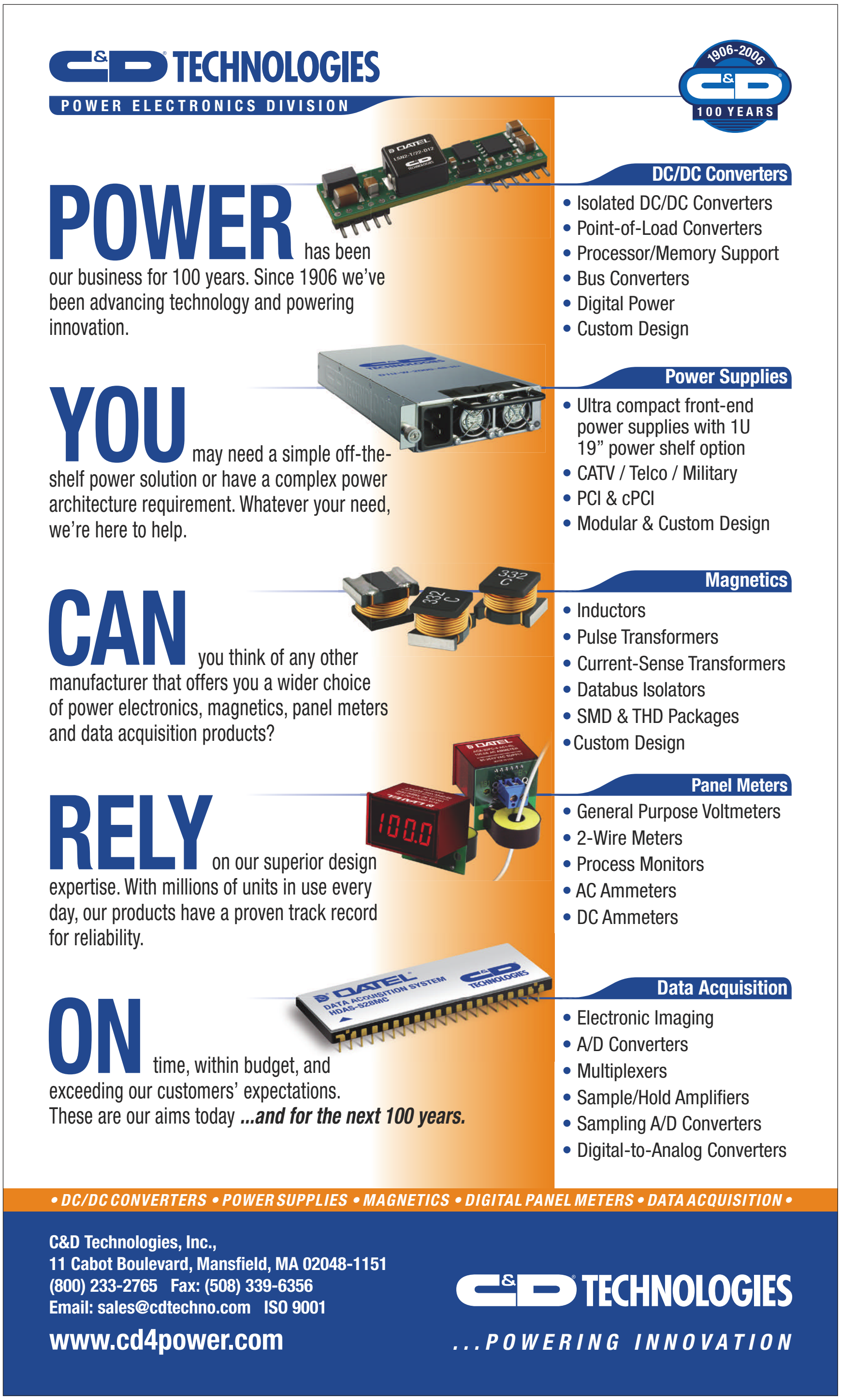

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LOOKING AHEAD

TO PCB DESIGN WEST

Despite all the automation, contractors, and board shops, pc-board design continues to be a critical step in bringing an electronic design to market. With growing challenges, including higher frequencies, greater demands on signal integrity, denser layouts with far more pins, and the use of remote board shops with limited capabilities, getting a board done right is never a given. It often becomes an engineering responsibility. The PCB Design Conference is arguably the grandfather of technical conferences in the field and is renowned for its training courses. The conference runs March 25 to 30, 2007, in the Santa Clara (CA) Convention Center.

LOOKING BACK

AS ELECTRONS PENETRATE THE WRIST WATCH

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—*Electrical Design News,* February 1957

LOOKING AROUND

AT ALL THAT HEAT WE GENERATE

Usually we think of heat in terms of resistive heating in circuits—something to model and control. But this time of year, at least in the Northern Hemisphere, it's easy to think of heat in terms of survival and comfort. And that brings up costs of fossil-fuel consumption, greenhouse gases, and efficiency. It's a pretty good prediction that as energy prices from burning natural resources rise, people will be willing to put more money—much more money—into systems that conserve heat in their homes and offices. For that matter, anyone who has calculated the cost of the drive train in a Toyota Prius can see this effect at work already on automotive efficiency. Despite the ballyhoo over consumer electronics, the source of sustained, profitable growth in electronics may actually be increasingly intelligent systems to improve the efficiency of our energy consumption.

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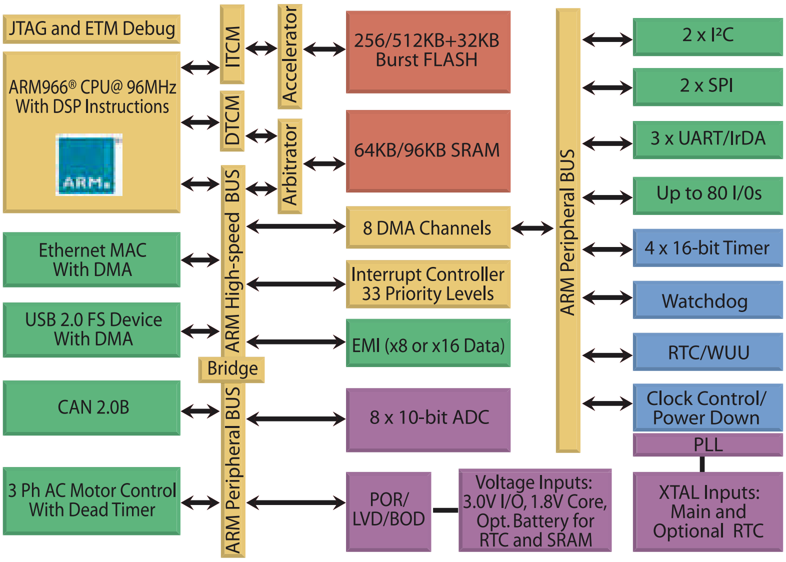

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